9000A-8048

Interface Pod

Instruction Manual

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NOTE

This manual documents the Model 9000A-8048 and its assemblies at the revision levels identified in Section 7. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdating information in Section 7 for older assemblies.

9000A-8048
Interface Pod

Instruction Manual

P/N 649418
SEPTEMBER 1982
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Section 1
Introduction

NOTE

It is assumed that the user of this manual is familiar with the basic operation of one of the 9000 Series Micro System Troubleshooters as described in the 9000 Series Operator manuals.

1-1. PURPOSE OF INTERFACE POD

The purpose of the 9000A-8048 Interface Pod (hereafter referred to as the pod) is to interface any 9000 Series Micro System Troubleshooter (hereafter referred to as the troubleshooter) to equipment employing a microcomputer of the 8048 or 8041 family. Table 1-1 lists the microcomputers currently supported by the pod. All devices operating with a clock frequency up to 11 MHz and within the normal operating temperature range of 0 to 50 degrees Celsius are supported.

The troubleshooter is designed to service printed circuit boards, instruments and systems employing microcomputers. The architecture of the troubleshooter is general in nature, and is designed to accommodate devices with up to 32 address lines and 32 data lines. The interface pod adapts the general purpose architecture of the troubleshooter to a specific microcomputer or microcomputer family. The pod adapts such microcomputer-specific functions as pin layout, status/control functions, interrupt handling, timing, and memory and I/O addressing.

1-2. DESCRIPTION OF POD

Figure 1-1 shows the communication between the pod, the troubleshooter, and the unit-under-test (hereafter referred to as the UUT). The pod connects to the troubleshooter through a shielded 24-conductor cable. The pod connects to the UUT through the microcomputer socket. The UUT microcomputer is removed from the UUT and replaced by the pod ribbon cable plug which gives the troubleshooter access to all system components which normally communicate with the microcomputer.

The external features of the pod are shown in Figure 1-2. If the microcomputer that is removed from the UUT is of the 8048 family, it is inserted into the socket exposed by the sliding door on the pod so that the pod can access ROM and RAM internal to the device (if a functioning UUT microcomputer is not available, any of the 8048 family microcomputers may be inserted into the socket; an 8039 microcomputer is included with the purchase of the pod). If the UUT is based on an 8041 family microcomputer, an 8048 family microcomputer must be installed in the microcomputer socket on the pod; the pod will not operate with an 8041 family microcomputer installed.

The pod consists of a pair of printed circuit board assemblies mounted within a break-resistant case. The pod contains an 8039 microcomputer along with the supporting hardware and control software that is required to do the following:

1. Perform handshaking with the troubleshooter.
2. Receive and execute commands from the troubleshooter.
3. Report UUT status to the troubleshooter.
4. Allow the UUT microcomputer to operate with the UUT.

The troubleshooter supplies operating power (+5V and -5V) for the pod. The UUT provides the external clock signal required by the pod for operation. Using the UUT clock signal allows the troubleshooter and pod to function at the designed operating speed of the UUT.

Logic level detection circuits are provided on each line to the UUT. These circuits allow detection of bus shorts, stuck-high or stuck-low conditions, and any bus drive conflict (two or more drivers attempting to drive the same bus line).

Over-voltage protection circuits are also provided on each line to the UUT. These circuits guard against pod damage which could result from the following:

1. Incorrectly inserting the ribbon cable plug in the UUT microcomputer socket.
2. UUT faults which place potentially-damaging voltages on the UUT microcomputer socket.

The over-voltage protection circuits guard against voltages of +12 to -7 volts on any one pin. Multiple faults, especially of long duration, may cause pod damage.

A power level sensing circuit constantly monitors the voltage level of the UUT power supply (+5V). If UUT power rises above or drops below an acceptable level the pod notifies the troubleshooter of the power fail condition.

A self test socket provided on the pod enables the troubleshooter to check pod operation. The self test socket is a 40-pin zero-insertion force type socket. The ribbon cable plug must be connected to the self test socket during self test operation. The ribbon cable plug should also be inserted into this socket when the pod is not in use to provide protection for the plug.

1-3. SPECIFICATIONS

Specifications for the pod are listed in Table 1-2.

Table 1-1. Products Supported by the 9000A-8048

MICROCOMPUTER FAMILY	MODEL NUMBERS SUPPORTED
8048	8035 8039 8040 8048 8049 8050 8748 8749
8041	8041 8041A 8042* 8741 8741A 8742*

NOTE: The pod is designed to match the characteristics of the original Intel family of NMOS microcomputers. Devices of other fabrication techniques (such as HMOS, XMOS, or CMOS) and of other manufacturers may differ in subtle ways. In general these devices are all compatible. Features such as selectively masked open drain outputs may, however, cause some difficulties. Components may have to be inserted into the circuit externally to simulate the action of open drain outputs.

Microsystems based on CMOS microcomputers may be tested with the troubleshooter and the pod provided that the supply voltage is nominally 5V and the clock speed is between 600 Hz and 11 MHz.

*The 8042 and 8742 microcomputers have a specified operating speed up to 12 MHz. However, because the pod operates with an 8048 family microcomputer installed, the maximum specified operating speed of the pod is 11.0 MHz.

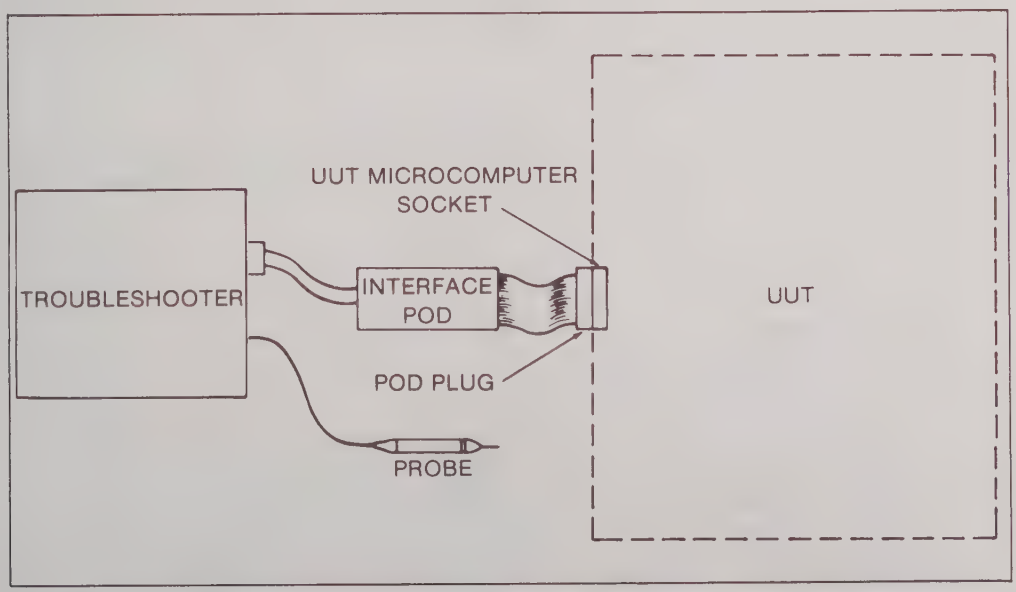

Figure 1-1. Communication Between the Troubleshooter, the Pod, and the UUT.

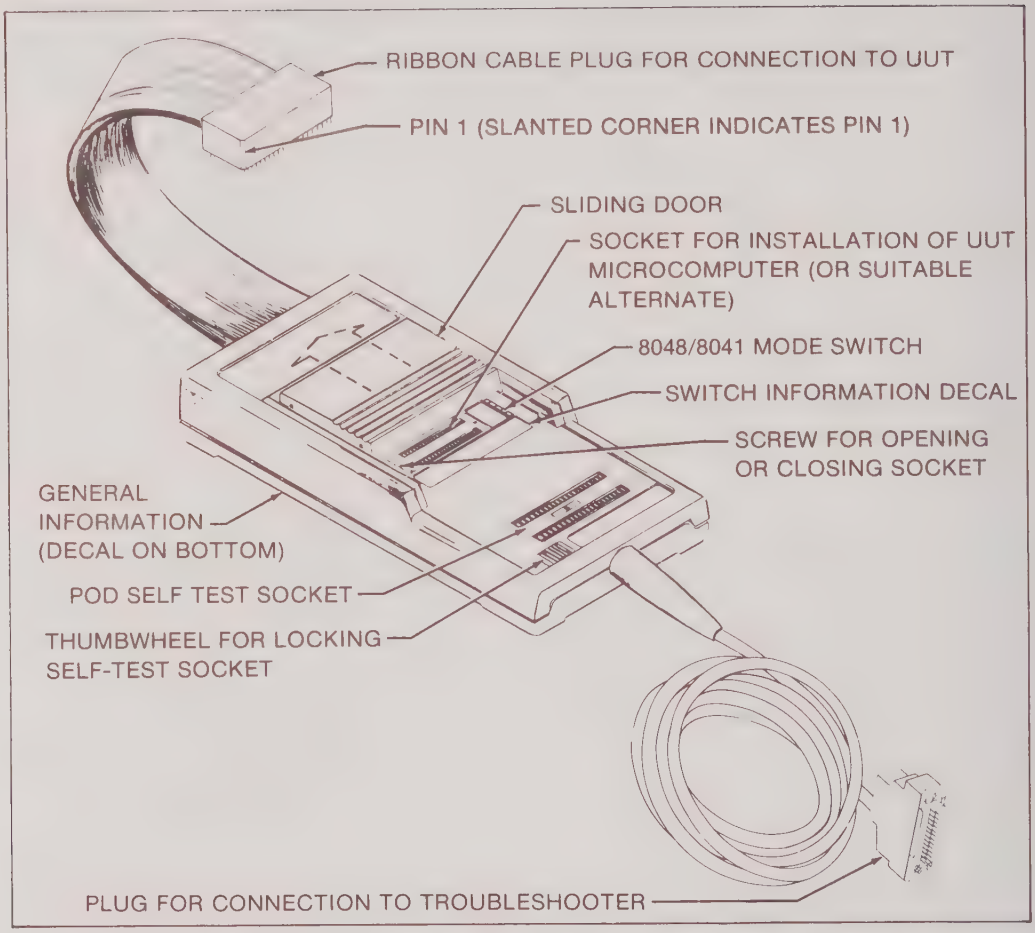
RIBBON CABLE PLUG FOR CONNECTION TO UUT
PIN 1 (SLANTED CORNER INDICATES PIN 1)
SLIDING DOOR
SOCKET FOR INSTALLATION OF UUT MICROCOMPUTER (OR SUITABLE ALTERNATE)
8048/8041 MODE SWITCH
SWITCH INFORMATION DECAL
SCREW FOR OPENING OR CLOSING SOCKET
GENERAL INFORMATION (DECAL ON BOTTOM)
POD SELF TEST SOCKET
THUMBWHEEL FOR LOCKING SELF-TEST SOCKET
PLUG FOR CONNECTION TO TROUBLESHOOTER

Figure 1-2. External Features of the 8048 Interface Pod.

Table 1-2. 8048 Pod Specifications

ELECTRICAL PERFORMANCE

Power Dissipation	6.0 watts maximum
Maximum External Voltage	-7 to +12 volts may be applied between ground and any ribbon cable plug pin continuously.

INTERFACE POD SIGNALS

Clock Input Low	0V min., +0.6V max
Clock Input High	+3.0V min., +5.0V max
Input Low Voltage	0V min., +0.8V max
Input High Voltage	+2.0V min., +5.0V max
Output Low Voltage	
P1, P2, TO	+0.45V max with Iol = 1.1 mA
ALL OTHER OUTPUT LINES	+0.4V max with Iol = 2.0 mA
Output High Voltage	+2.4V min. with Ioh = -400 uA
Tristate Output Leakage Current	±20 uA
High Level Input Current	20 uA (typ.) with Vih = +2.7V

Table 1-2. 8048 Pod Specifications (cont)

INTERFACE POD SIGNALS (cont)	
Low Level Input Current	
P1, P2, SS, EA	-200 uA (typ.) with Vil = +0.4V
ALL OTHER INPUT LINES	-20 uA (typ.) with Vil = +0.4V
TIMING CHARACTERISTICS	
Maximum Clock Frequency	11.0 MHz (dependent on UUT)
Added Delays to 8048 Signals	
LOW-TO-HIGH TRANSITIONS	30 ns typical
HIGH-TO-LOW TRANSITIONS	30 ns typical
UUT POWER DETECTION	
Detection of Low Vcc Fault	Vcc < +4.5V
Detection of High Vcc Fault	Vcc > +5.5V
Pod Protection from UUT Low Power*	Vcc < +3.5V
GENERAL	
Size	5.7 cm H x 14.5 cm W x 27.1 cm L (2.2 in H x 5.7 in W x 10.7 in L)
Weight	1.4 kg (3.1 lbs.)
Environmental	
STORAGE	-40°C to +70°C, RH <95%
OPERATING	0°C to +25°C, RH <95% +25°C to +40°C, RH <75% +40°C to +50°C, RH <45%
Protection Class 3	Relates solely to insulation or grounding properties defined in IEC 348.

*Pod outputs tristate and/or drive lines to low logic level.

Section 2
Installation and Self Test

2-1. INTRODUCTION

The procedures for performing the pod self test and connecting the pod to the troubleshooter and the UUT are given in the following paragraphs.

2-2. PERFORMING THE POD SELF TEST

In order to perform the pod self test, an 8048 family microcomputer must be installed in the pod and the pod must be connected to the troubleshooter. Perform the following steps:

1. Remove power from the UUT and the troubleshooter.

2. If the UUT microcomputer is of the 8048 family, disassemble the UUT and remove the UUT microcomputer from its socket. Install the UUT microcomputer in the pod socket at the location shown in Figure 2-1. If the UUT microcomputer is of the 8041 family, install any 8048 family microcomputer. (An 8039 microcomputer is included with the purchase of the pod.) The pod socket is opened or closed by using a screwdriver to turn the screw at the end of the socket. Turn the screw counterclockwise to open the socket, and clockwise to close the socket.

3. Place the mode switch indicated in Figure 2-1 to the correct position as indicated on the decal beside the mode switch. Refer to Table 2-1 for a list of microcomputer types and the correct mode switch setting.

4. Open the pins of the pod self test socket by operating the adjacent thumbwheel. Insert the ribbon cable plug into the socket and close the socket using the thumbwheel.

5. Using the round shielded cable, connect the pod to the troubleshooter at the location shown in Figure 2-2. Secure the connector using the sliding collar.

6. Apply power to the troubleshooter.

7. Press the BUS TEST key to initiate the pod self test.

If the troubleshooter displays the message *POD SELF TEST name OK*, then the pod is operating properly. (The word *name* corresponds to the microcomputer model number. For the 8048 family microcomputers, the pod is able to detect and display the model number of the microcomputer installed in the pod; for the 8041 family microcomputers, the pod reports the name 8041. Refer to Table 2-1 for the display message corresponding to each model number.)

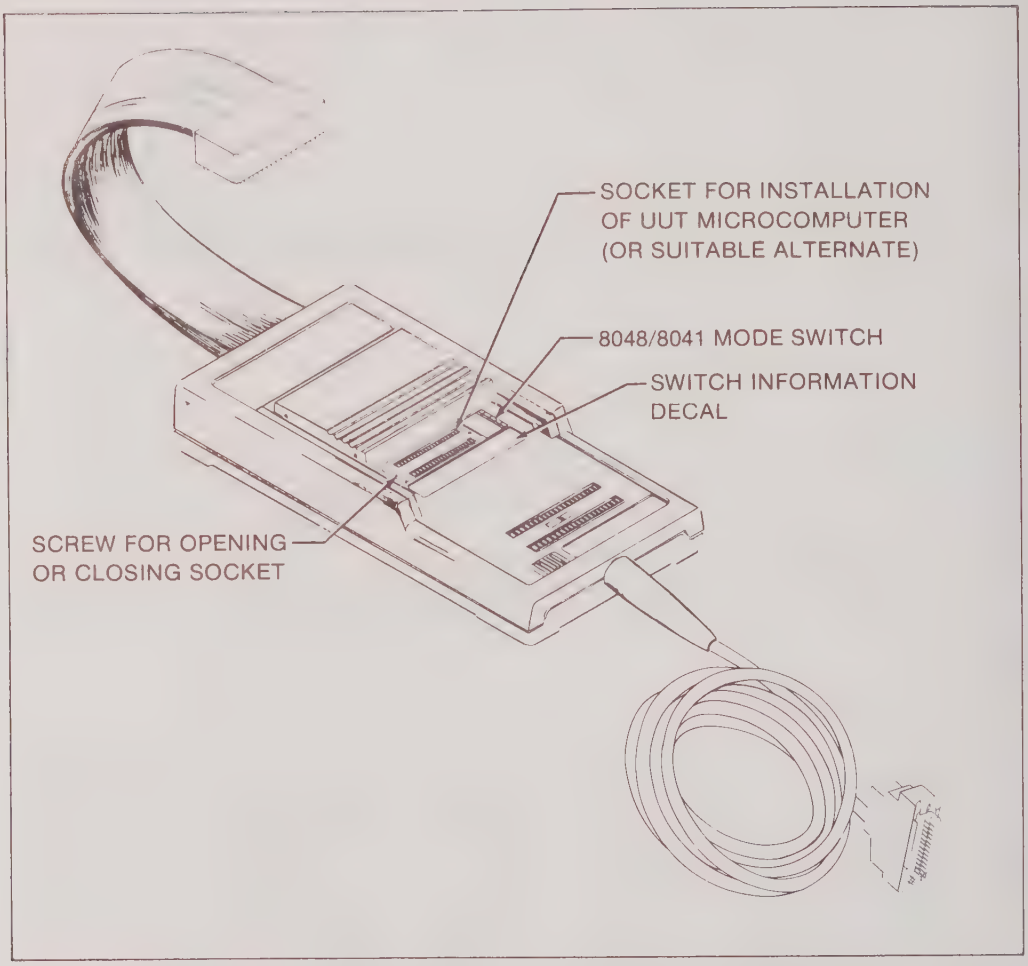

Figure 2-1. Location of Microcomputer Socket and Mode Switch

If the troubleshooter displays the message *POD SELF TEST* name *FAIL xx*, or if the name reported does not correspond to the microcomputer model number installed and the mode switch setting, the pod may not be operating properly. (The letters *xx* correspond to a failure code describing the error; the failure codes are listed in Section 6.) If the UUT microcomputer has been installed in the pod, the UUT microcomputer may be causing the failure. Replace the UUT microcomputer with a suitable alternate and try the self test again. Make sure the microcomputer is properly positioned in the self test socket before trying the test.

For information about pod troubleshooting and repair, refer to Section 6.

2-3. CONNECTING THE POD TO THE UUT

WARNING

TO PREVENT POSSIBLE HAZARDS TO THE OPERATOR OR DAMAGE TO THE UUT, DISCONNECT ALL HIGH-VOLTAGE POWER SUPPLIES, THERMAL ELEMENTS, MOTORS, OR MECHANICAL ACTUATORS WHICH ARE CONTROLLED OR PROGRAMMED BY THE UUT MICROCOMPUTER BEFORE CONNECTING THE POD.

Connect the pod between the troubleshooter and the UUT as follows:

1. Be sure that power is removed from the UUT.

2. Disconnect UUT analog outputs or potentially hazardous UUT peripheral devices as described in the warning at the beginning of this section.

3. Disassemble the UUT to gain access to the UUT microcomputer socket. If the UUT microcomputer is still in the socket, remove the microcomputer.

4. Turn the pod self test socket thumbwheel to release the pod plug, and remove the pod plug from the self test socket.

5. Insert the pod plug into the UUT microcomputer socket. Make sure the slanted corner of the pod plug is aligned with pin 1 of the UUT microcomputer socket.

6. Reassemble the UUT using extender boards if necessary.

CAUTION

To prevent damage to the pod, ensure that troubleshooter power is on before turning UUT power on in order to activate protection circuits within the pod.

7. Apply power to the UUT.

Table 2-1. 8041/8048 Message Name and Mode Switch Setting

UUT MICROCOMPUTER TYPE	NAME DISPLAYED BY TROUBLESHOOTER*	MODE SWITCH SETTING
8035 8048 8748	*'35/48*	8048 MODE
8039 8049 8749	*'39/49*	
8040 8050	*'40/50*	
8041 8041A 8741 8741A 8042 8742	*8041*	8041 MODE

*The *name* is displayed by the troubleshooter in the pod self test messages *POD SELF TEST name OK* or *POD SELF TEST name FAIL xx*.

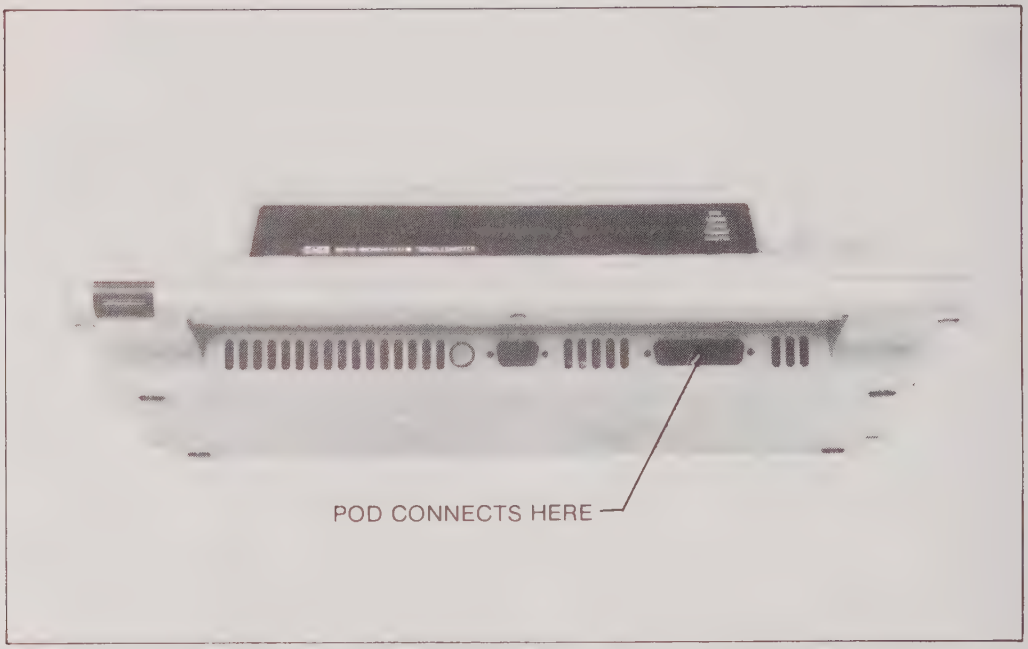

Figure 2-2. Connection of Interface Pod to Troubleshooter

Section 3
Microcomputer Data

3-1. INTRODUCTION

This section contains microcomputer data which may be useful during operation of the troubleshooter. This information includes descriptions of 8048 and 8041 signals and pin assignments.

3-2. MICROCOMPUTER SIGNALS

Table 3-1 lists all of the 8048 family microcomputer signals and provides a brief description of each. Table 3-2 provides similar information for the 8041 family of microcomputers. Figure 3-1 shows the 8048 pin assignments and Figure 3-2 shows the 8041 pin assignments.

Table 3-1. 8048 Microcomputer Signals

SIGNAL NAME	DESCRIPTION
DB0-DB7	This eight-line bus serves as a multiplexed data and address (low-order eight bits) bus. In devices capable of program execution out of internal ROM, this bus may serve also as a bidirectional I/O port or static latch when no external data or program memory accesses are occurring. As an output port, data on this bus remains latched until the next output. Bus operations other than the following operations cause DB0-DB7 to revert to the high-impedance state: OUTL BUS,A ANL BUS,#DATA ORL BUS,#DATA, INS A,BUS
P10-P17 (Port 1)	This eight-line bus serves as a quasi-bidirectional I/O port. As an output port, data on this bus is fully latched. As an input port, external logic presenting the data must pull the individual lines from a high to a low level. As a result, a high level must be written to each line which is to be used as an input. External logic cannot create a high level at any of these lines which output a low level.

Table 3-1. 8048 Microcomputer Signals (cont)

SIGNAL NAME	DESCRIPTION
P20-P23 and P24-P27 (Port 2)	This eight-line bus performs up to three functions: 1. An eight-line I/O port as described for lines P10-P17. 2. Lines P20-P23 multiplex the high-order four bits of address (A8-A11) during external program memory operations, along with I/O data. 3. Lines P20-P23 serve as a four-bit expander bus during I/O expander operations with an 8243 I/O expander and the PROG output. These operations allow access to Ports P4-P7.
$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ input is held low for a minimum of five machine cycles (10 ms during power-up) to: 1. Set the program counter to zero. 2. Set the stack pointer to zero. 3. Select register bank zero. 4. Select memory bank zero. 5. Set ports 1 and 2 to input mode. 6. Set DB0-DB7 to high impedance state. 7. Disable interrupts (timer and external). 8. Stop timer. 9. Clear timer flag. 10. Clear F0 and F1 flags. 11. Set T0 to input mode.
$\overline{\text{SS}}$	A logic low at the $\overline{\text{SS}}$ (single step) input is used in conjunction with the ALE output to single step the microcomputer through a program.
XTAL1, XTAL2	Two inputs which permit connection of a crystal for use by the internal clock circuit. An external clock source having complementary outputs may be connected in place of the crystal.
EA	A logic high at the EA (external address) input causes all program memory fetches to address external memory (all devices which contain no program ROM must use this input). The $\overline{\text{RESET}}$ input must be low when changing the state of the EA line.
T0	The T0 line may be used as a test input sampled by conditional branch instruction. The T0 line may be designated by software as a clock output at 1/3 of the crystal frequency. A low $\overline{\text{RESET}}$ input reverts the T0 line back to a test input.
T1	The T1 line may be used as a test input sampled by conditional branch instructions. The T1 line may, under software control, be used as a count input to an internal counter/timer.

Table 3-1. 8048 Microcomputer Signals (cont)

SIGNAL NAME	DESCRIPTION
PROG	As an input, PROG enables the application of programming pulses during the programming of devices which contain EPROM (programming operations are not emulated by the pod). As an output, PROG is used in conjunction with the expander bus (P20-P23) during 8243 I/O expander operations. A high-to-low transition output on the PROG line indicates the presence of a four-bit op code on the expander bus. The following low-to-high transition on the PROG line is used to strobe data on or off the expander bus, depending whether the operation is a read or write.
$\overline{RD}$	The $\overline{RD}$ (read) output is made low to strobe data onto the DB0-DB7 bus during read operations from an external device or RAM.
$\overline{WR}$	The $\overline{WR}$ (write) output is made low to strobe data from the DB0-DB7 bus during write operations into an external device or RAM.
ALE	The ALE (address latch enable) output occurs once per machine cycle. The low-to-high transition indicates the presence of I/O data on lines P20-P23. The high-to-low transition indicates that a valid address may be on the DB0-DB7 bus, and also on lines P20-P23 if an external program fetch is in progress. When single-stepping the microcomputer through a program, ALE goes high (and remains high as long as $\overline{SS}$ is low) to indicate that the program counter contents are present on DB0-DB7 and P20-P23.
$\overline{PSEN}$	The $\overline{PSEN}$ (program store enable) output is made low to strobe (read) the contents of external program memory onto the DB0-DB7 bus.
$\overline{INT}$	A high-to-low transition at this input initiates the interrupt handling sequence if interrupts have been enabled through software. The $\overline{INT}$ line may be used as a test input sampled by a conditional branch instruction.
Vdd	The Vdd pin is normally used as a low power standby supply for the internal RAM of the microcomputer. Some manufacturers have redesigned the 8048 so that this input is used as a logic input which causes the microcomputer to enter a low power standby mode. The pod considers this line to be a power supply input and may report a power fail condition if the voltage at this pin is not +5V. With UUTs that use this pin as a logic input, measures should be taken to ensure that the signal is logic high during testing (an external pull-up resistor may be necessary) to avoid false reporting of UUT power fail.

Table 3-2. 8041 Microcomputer Signals

SIGNAL NAME	DESCRIPTION
D0-D7	These eight lines provide a tri-state bidirectional data bus connection to an eight-bit system bus.
P10-P17 (Port 1)	This eight-line bus serves as a quasi-bidirectional I/O port. As an output port, data on this bus is fully latched. As an input port, external logic presenting the data must pull the individual lines from a high to a low level. As a result, a high level must be written to each line which is to be used as an input. External logic cannot create a high level at any of these lines which output a low level.
P20-P23 and P24-P27 (Port 2)	This eight-line bus performs two functions: 1. An eight-line I/O port as described for lines P10-P17. 2. Lines P20-P23 serve as a four-bit expander bus during I/O expander operations with an 8243 I/O expander and the PROG output.
$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ input is held low for a minimum of five machine cycles (50 ms during power-up) to: 1. Set the program counter to zero. 2. Set the stack pointer to zero. 3. Select register bank zero. 4. Set ports 1 and 2 to input mode. 5. Disable timer interrupt. 6. Stop timer. 7. Clear timer flag. 8. Clear F0 and F1 flags.
$\overline{\text{SS}}$	A logic low at the $\overline{\text{SS}}$ (single step) input is used in conjunction with the SYNC output to single step the microcomputer through a program.
XTAL1,XTAL2	Two inputs which permit connection of a crystal for use by the internal clock circuit. An external clock source having complementary outputs may be connected in place of the crystal.
EA	A logic high at the EA (external address) input activates the program verify mode (not implemented by pod).
T0	The T0 line may be used as a test input sampled by conditional branch instructions. With the $\overline{\text{RESET}}$ line low and the EA line high, the T0 may be made high to allow addressing of internal program memory of those devices so equipped (not implemented by pod).
T1	The T1 line may be used as a test input sampled by conditional branch instructions. The T1 line may, under software control, be used as a count input to an internal counter/timer.
PROG	As an input, PROG enables the application of programming pulses during the programming of devices which contain EPROM (not implemented by pod).

Table 3-2. 8041 Microcomputer Signals (cont)

SIGNAL NAME	DESCRIPTION
PROG (cont.)	As an output, PROG is used in conjunction with the expander bus (P20-P23) during 8243 I/O expander operations. A high-to-low transition output on the PROG line indicates the presence of a four-bit op code on the expander bus. The following low-to-high transition on the PROG line is used to strobe data on or off the bus, depending whether the operation is a read or write.
$\overline{RD}$	The $\overline{RD}$ (read) input is made low by a master processor in order to read data and status words from the 8041 via the D0-D7 bus.
$\overline{WR}$	The $\overline{WR}$ (write) input is made low by a master processor in order to write data and command words to the 8041 via the D0-D7 bus.
SYNC	When single-stepping the microcomputer through a program, SYNC goes high (and remains high as long as $\overline{SS}$ is low) to indicate that the program counter contents are present on D0-D7 and P20-P23. SYNC output occurs once per machine cycle. In normal operation, the SYNC output may also be used to clock external circuitry.
A0	The A0 input is used by the master processor to indicate whether the byte transfer over the D0-D7 bus is data or command.
$\overline{CS}$	The $\overline{CS}$(chip select) input is used to select one microcomputer out of several connected to a common data bus.

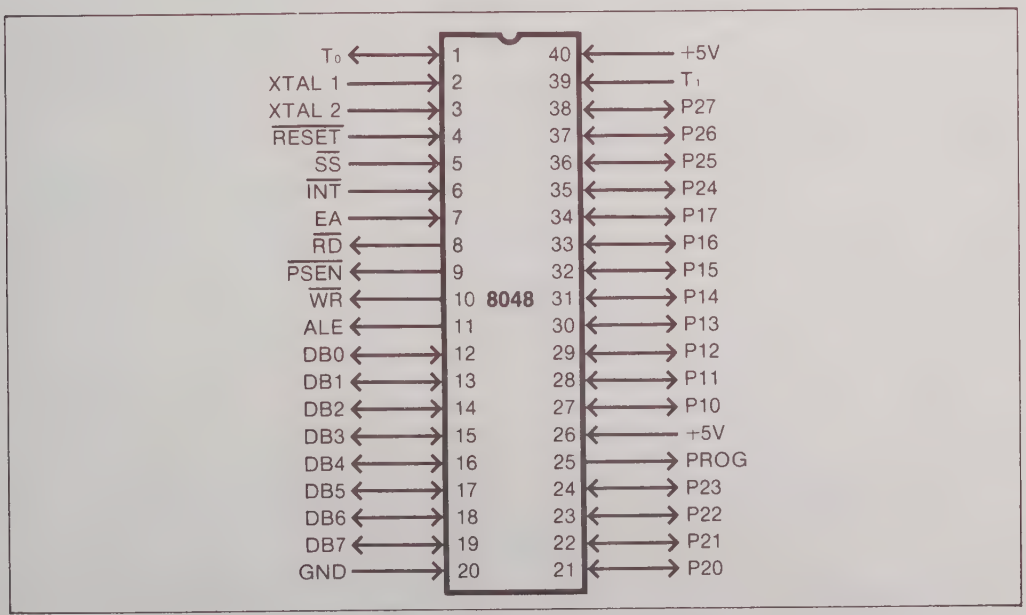

Figure 3-1. 8048 Pin Assignments

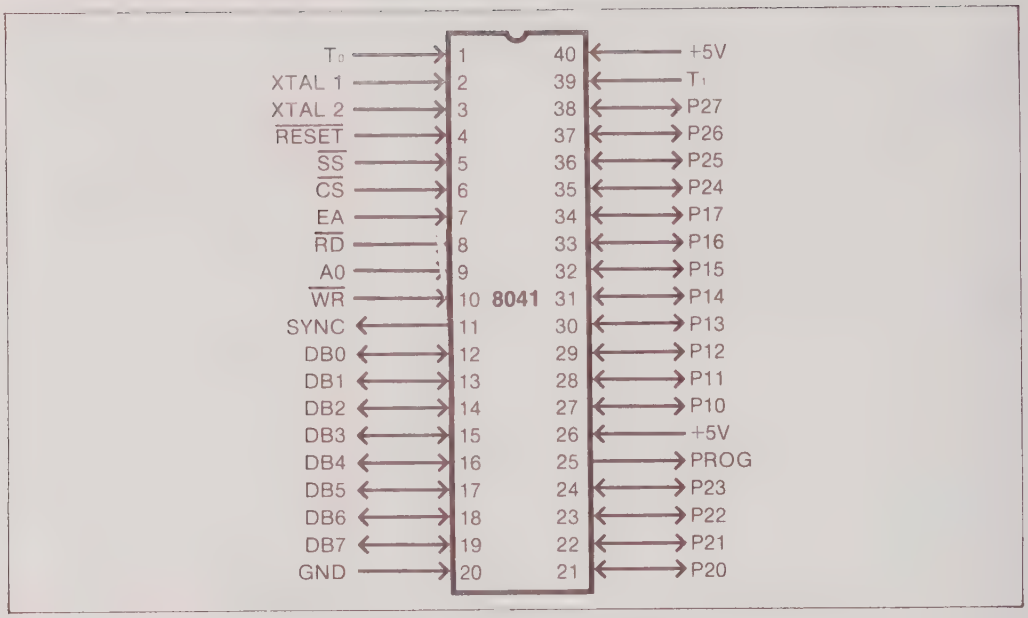

Figure 3-2. 8041 Pin Assignments

Section 4
Operating Characteristics

4-1. INTRODUCTION

This section contains information which pertains to operating the troubleshooter with systems employing the 8048 or 8041 microcomputer families. Information provided is in addition to and complements that provided in the troubleshooter operator and programming manuals, and covers such items as the following:

- Definition and bit assignment of status lines
- Definition of forcing and interrupt lines
- Bit assignment of control lines
- Address space assignment
- Access to program memory, RAM, registers, stack, and ports
- Characteristics of Learn and Bus Test operations
- Quick Looping read and write functions unique to 8048/8041 pod
- Marginal UUT problems

4-2. STATUS/CONTROL LINES

4-3. Introduction

The pod provides the interface between the general architecture of the troubleshooter and the specific design features of the UUT. As part of this interface task, the pod makes specific assignments between the UUT microcomputer lines and the troubleshooter. These assignments include the following:

- Bit number assignment of status lines
- Bit number assignment of control lines
- Address space assignment
- Pin assignments

These assignments are described in the following paragraphs, and are summarized on a decal on the bottom of the pod.

4-4. Status Line Bit Assignments

When a Read Status operation is performed, the troubleshooter displays the result in binary form, where "1" indicates a logic high status line and a "0" indicates a logic low

status line. To determine which characters of the display correspond to specific status lines, refer to Table 4-1. Table 4-1 shows that each line is assigned a bit number. On the troubleshooter display, bit zero appears at the far right side of the display, while bit 11 (when used) appears at the far left.

For both the 8048 and 8041 families of microcomputers, the lowest numbered status line is bit zero, which is the $\overline{SS}$ (single-step) line. For the 8048 family, the highest numbered status line is bit 7, which is the PWR FAIL (power fail) line. For the 8041 family, the highest numbered status line is bit 11, which is the A0 line.

For example, if a Read Status operation is performed with an 8048-based system and the $\overline{SS}$ (bit number 0) and PWR FAIL (bit number 7) lines are low and all other status lines are high, the troubleshooter will display the message *READ@STS=0011 1110 OK.* In this example bit numbers 0 (SS) and 7 (PWR FAIL) are zero to indicate a logic low, while other meaningful bits are ones to indicate logic high. Bit 6, which has no meaning as an 8048 status line, is always represented by zero. Bits 8 through 11 are not displayed for 8048-based systems. Bits 6 and 10, which have no meaning as 8041 status lines, are always represented by zeros in the troubleshooter display message for 8041-based systems.

NOTE

The Power Fail bit does not represent a particular 8048 or 8041 signal, but is generated within the pod whenever UUT voltage levels deviate from acceptable limits.

4-5. Control Line Bit Assignments

The pod does not allow the troubleshooter to write directly to any of the microcomputer control lines with the Write Control or Data Toggle Control functions. However, all 8048 and 8041 control lines listed in Tables 3-1 and 3-2 are tested by means of the troubleshooter Bus Test.

Table 4-1. Status and Control Line Bit Assignments

STATUS LINES			CONTROL LINES		
BIT NUMBER	SIGNAL		BIT NUMBER	SIGNAL	
	8048	8041		8048	8041
11	—	A0	7	$\overline{PSEN}$	—
10	—	—	6	—	—
9	—	$\overline{WR}$	5	$\overline{WR}$	—
8	—	$\overline{RD}$	4	$\overline{RD}$	—
7	PWR FAIL	PWR FAIL	3	PROG	PROG
6	—	—	2	—	—
5	EA	EA	1	T0(CLK)	—
4	**$\overline{RESET}$	**$\overline{RESET}$	0	ALE	SYNC
3	$\overline{INT}$	**$\overline{CS}$			
2	T1	T1			
1	T0	T0			
0	**$\overline{SS}$	**$\overline{SS}$			

**Forcing Lines

When performing a Bus Test, if a control line cannot be driven, the troubleshooter displays the message *CTL ERR xxxxxxxx-LOOP?* The string *xxxxxxxx* represents a binary string that identifies which lines can or cannot be driven. A 1 indicates the corresponding line cannot be driven, while a 0 indicates the corresponding line can be driven. For example, if the $\overline{\text{PSEN}}$ line of an 8048 cannot be driven, but all other control lines can be driven, the troubleshooter displays the message *CTL ERR @ 10000000 LOOP?* (the $\overline{\text{PSEN}}$ line is represented by bit number 7). Table 4-1 lists all control lines and their respective bit numbers.

4-6. FORCING AND INTERRUPT LINES

Several troubleshooter messages are used to indicate errors and conditions associated with forcing lines and interrupts. Forcing lines are those lines which, when made active, force the microcomputer into some specific action. Forcing lines for the 8048 family of microcomputers are $\overline{\text{Reset}}$ and $\overline{\text{SS}}$. Forcing lines for the 8041 family are $\overline{\text{Reset}}$, $\overline{\text{CS}}$, and $\overline{\text{SS}}$. The interrupt line for the 8048 family is the $\overline{\text{INT}}$ line. The 8041 family provides no external interrupt features.

The $\overline{\text{Reset}}$, $\overline{\text{SS}}$, and $\overline{\text{INT}}$ lines are functionally enabled only when the troubleshooter is operated in the Run UUT mode (where the pod emulates the UUT microcomputer). In all other operating modes, the troubleshooter monitors the control lines and may cause active forcing or interrrupt line messages to appear on the troubleshooter display.

The reporting of active forcing lines or active interrupt lines may be disabled with the Setup operation on the troubleshooter. If the $\overline{\text{Reset}}$ line is pulled low, the pod reports such a condition to the troubleshooter, but pod operation is unaffected.

4-7. ADDRESS SPACE ASSIGNMENT

4-8. Introduction

The 8048 and 8041 families of microcomputers are capable of addressing some or all of the memory and I/O functions listed and described briefly in Table 4-2. Additional information about microcomputer access to address space is provided in the following paragraphs.

4-9. Access to External Program Memory (8048 Family Only)

Program memory external to the microcomputer (in the UUT) occupies address space 0000 - 0FFF. The external program memory is usually ROM, EPROM, or RAM, and is all considered read-only memory. Any read operations in this address space exercise the address lines, data lines, and the $\overline{\text{PSEN}}$ control line (read operations in this address space are illustrated in Figure 4-1). Since this address space is defined as read-only, an attempted write operation reports that no data lines are drivable.

4-10. Access to Internal RAM, Registers, and Stack

Internal RAM, including the working registers and stack of the UUT microcomputer, is accessible in the address space 1000 - 10FF. The amount of RAM in this address space varies from 64 to 256 bytes, depending upon the UUT microcomputer present in the pod socket. If the microcomputer contains less than 256 bytes of RAM, memory wrap-around occurs and the same locations appear at higher memory addresses.

Access to the UUT microcomputer RAM allows the user to initialize variables and working registers prior to operation of the troubleshooter in the Run UUT mode.

4-11. Access to External Data Memory (8048 Family Only)

Data memory external to the microcomputer (in the UUT) occupies address space 1100 - 11FF. This address space is read/writeable and generally contains RAM, memory-mapped I/O, or a variety of peripheral devices. A read operation in this address space exercises the multiplexed address/data bus (DB0 - DB7) and the $\overline{\text{RD}}$ control line. A write operation in this address space exercises the bus and the $\overline{\text{WR}}$ control line. Read and write operations in this address space correspond to the microcomputer instructions MOVX

A,@Rn and MOVX @Rn,A respectively. Read and write operations in this address space are illustrated in Figure 4-2.

4-12. Access to the 8048 Bus Port (DB0 - DB7)

The eight-line bidirectional bus port (DB0 - DB7) is addressed at location 2000 (access to the bus port is illustrated in Figure 4-3). In a minimal system configuration, an 8048 uses only internal memory; the bus port is used as a bidirectional I/O port. In this configuation, a read operation at location 2000 results in only exercising the $\overline{RD}$ control line. Unlike read operations at addresses in the address space 1100 - 11FF (external data memory), read operations at address 2000 do not multiplex address and data on the bus port. Read operations are equivalent to the INS A,BUS instruction.

A write operation to location 2000 presents data to the bus port and exercises the $\overline{WR}$ control line, but does not output any address information. In addition, the write operation latches the data at the bus port. The data remains latched until another operation occurs which requires address information to be multiplexed on the bus. Write operations are equivalent to the OUTL BUS,A instruction.

Table 4-2. Address Space Assignment

ADDRESS	FUNCTION ADDRESSED
0000-0FFF*	External Program Memory. This is usually ROM within the UUT. These addresses correspond to the real addresses 000-FFF (internal microcomputer ROM, when present, is not accessible by the troubleshooter; however, Run UUT at internal addresses is possible).
1000-10FF	Internal RAM, Registers and Stack. Up to 256 bytes may be addressed, depending upon the device used in the UUT. The addresses correspond to the real internal eight-bit addresses, 00 - FF, which include the working registers and stack.
1100-11FF*	External Data Memory. This is usually RAM or I/O located on the UUT data bus. This address space corresponds to the real external data memory addresses, 00-FF.
2000	Bus Port. In minimal systems, the microcomputer data bus may be configured as a bidirectional I/O port (8048 outputs remain latched until the next UUT access operation occurs which requires use of the data bus).
2001-2002	Port 1 and Port 2. The two eight-bit I/O ports (ports 1 and 2) of the microcomputer may be read from and written to at these addresses.
2004-2007	Expander I/O Ports. Any of the 8243 expander I/O ports (ports 4 through 7) may be read from and written to at these addresses.
3000-30FF	Executable Pod RAM. Up to 256 bytes of RAM contained within the pod may be read from and written to at these addresses. This RAM is provided for the user to write short test routines.
4000*	T0 Line. Writing 01 to this address sets the T0 line as a clock output; writing 00 sets it as an input. A read at this address yields the setting (configuration) of the T0 line.

*8048 family only.

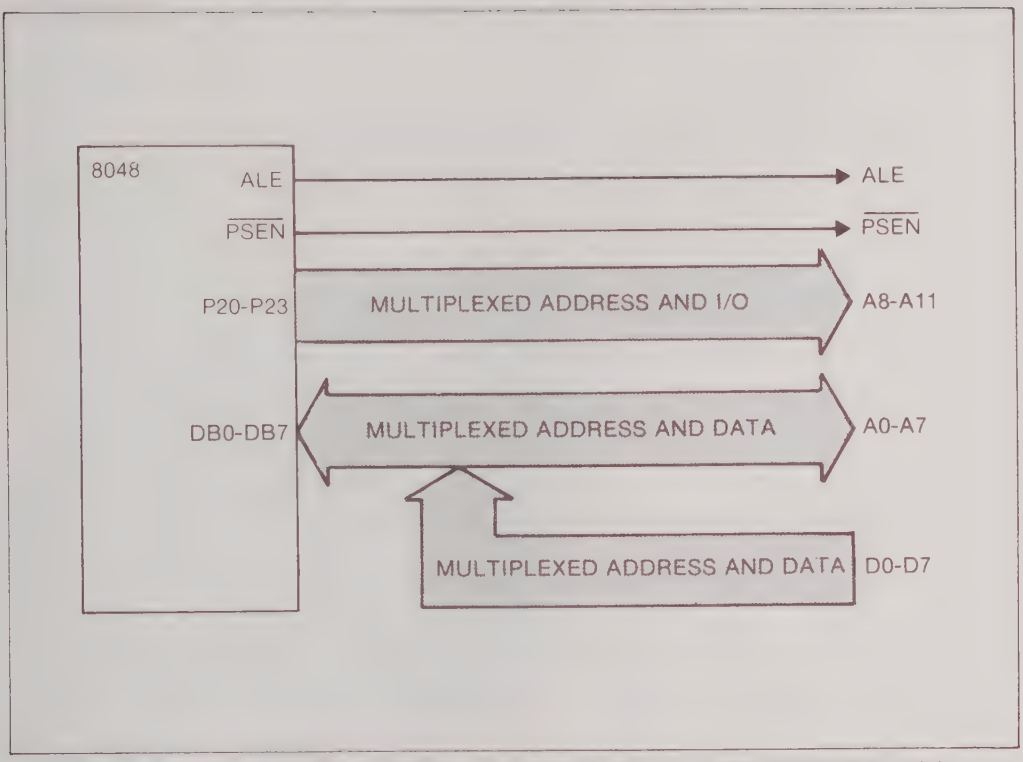

Figure 4-1. Reading External Program Memory Addresses 0000-0FFF (8048 only)

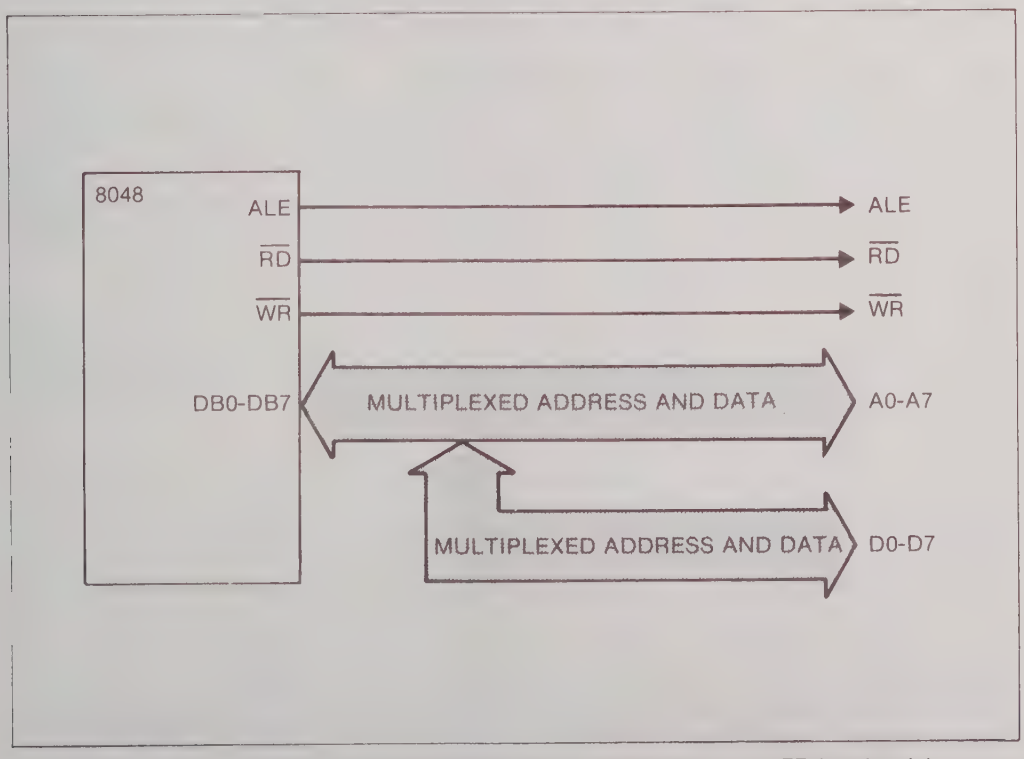

Figure 4-2. Access to External Data Memory Addresses 1100-11FF (8048 only)

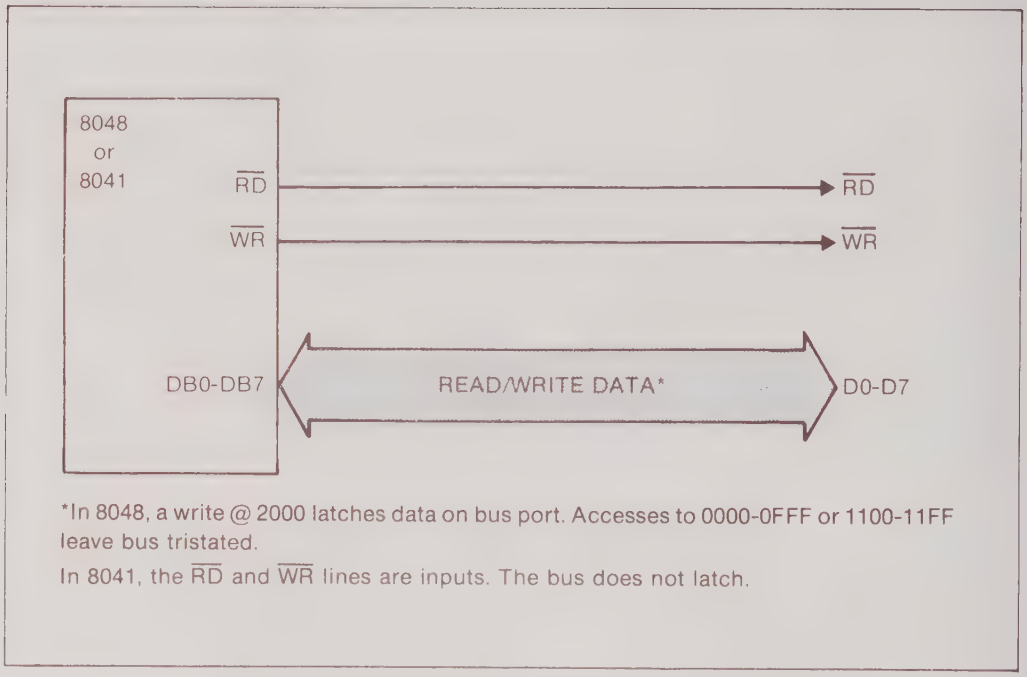

Figure 4-3. Access to 8048 or 8041 Bus Port (Address 2000)

Troubleshooter operations which cause the bus to revert to the high-impedance state are read operations in the address space 000-FFF, and read or write operations in the address space 1100-11FF. A read operation at location 2000 does not affect data latched at the bus port (the latched data is actually what is read).

4-13. Access to the 8041 Bus Port (DB0-DB7)

The eight-line bidirectional bus port (DB0 - DB7) is addressed at location 2000 (access to the bus port is illustrated in Figure 4-3). Momentary access to the 8041 data bus may be made by means of this address. Written data is applied to the data bus only for a short duration and is not latched as in the 8048 family of devices. This is sufficient for making checks with the troubleshooter probe, and for the pod to verify the drivability of the bus.

4-14. Access to Ports 1 and 2

The two eight-line quasi-bidirectional ports, Ports 1 and 2, are addressed at locations 2001 and 2002 respectively (access to the ports is illustrated in Figure 4-4). The lines of these ports can be individually configured as inputs or outputs. Writing a bit high sets the corresponding line as an input. All bits are initially high upon reset.

Write operations output the specified data to the addressed port where it remains latched until a subsequent write operation or reset is performed. Read operations obtain the state of the latched outputs and the state of the input lines which were previously written high. Write operations are equivalent to the OUTL Pn,A instruction. Read operations are equivalent to the IN A,Pn instruction. No control lines are associated with operations on Ports 1 and 2.

Any attempt to write to lines configured as inputs may cause drivability errors to appear on the troubleshooter display. Write operations are a part of the Learn and Bus Test functions of the troubleshooter, and drivability errors which occur due to lines configured as inputs may be disregarded.

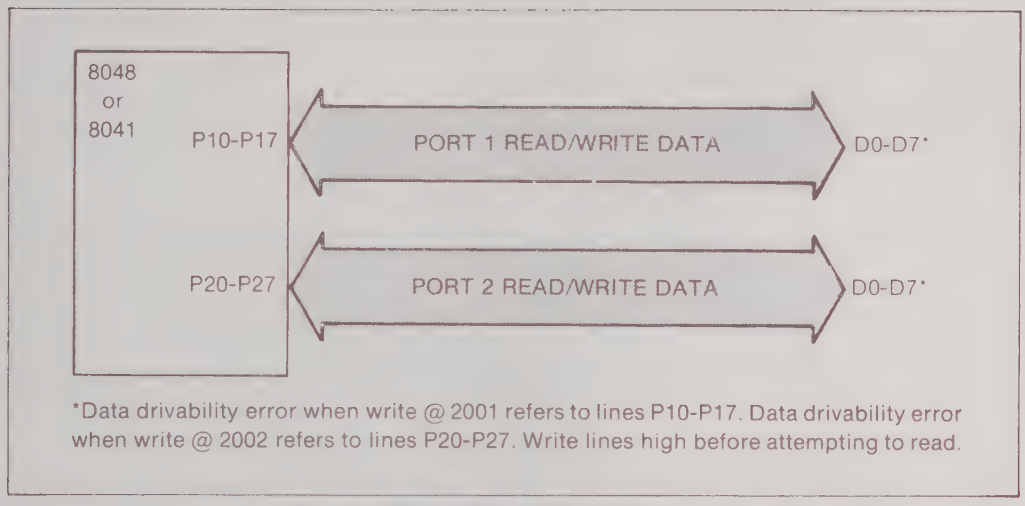
8048
or
8041
P10-P17
PORT 1 READ/WRITE DATA
D0-D7*
P20-P27
PORT 2 READ/WRITE DATA
D0-D7*
*Data drivability error when write @ 2001 refers to lines P10-P17. Data drivability error when write @ 2002 refers to lines P20-P27. Write lines high before attempting to read.

Figure 4-4. Access to Ports 1 and 2 (Addresses 2001 and 2002)

NOTE

Any data drivability errors which occur during accesses to location 2001 and 2002 indicate errors on the lines of either Port 1 or Port 2, and not the data bus DB0-DB7.

4-15. Access to Expander I/O Ports

The four expander I/O ports (P4 - P7) of a UUT-mounted 8243 may be accessed using addresses 2004 through 2007 (access to the ports is illustrated in Figure 4-5). As a result, any of the expander I/O devices (connected to Ports 4 through 7) may be accessed by means of read and write operations in this address space. Read and write operations in this address space exercise the I/O expansion bus (P20 - P23) and PROG line.

Address drivability errors may occur during a read or write operation if the I/O expander bus (P20 - P23) is not drivable with the multiplexed address/instruction code information. Data drivability errors may occur during a write operation if the I/O expander bus (P20-P23) is not drivable with the written data. Write operations are equivalent ot the MOVD Pn,A instruction. Read operations are equivalent to the MOVD A,Pn instruction. Address and data drivability errors may also occur if the I/O expansion bus is configured to be used in an input mode only.

Often, a UUT contains two or more I/O expander devices. Selection of a particular I/O expander is usually accomplished by writing the appropriate data to one or more of the other 8048 ports.

4-16. Access to Pod RAM

Up to 256 bytes of pod-resident RAM may be accessed in the address space 3000 - 30FF. This RAM provides executable memory to the user for the purpose of writing and executing short test routines. The contents of this RAM are executed as if they were internal to the microcomputer (as its own ROM) at real addresses X00 - XFF (X = any hex digit). During execution, all program memory fetches access this memory, while all data memory references access the UUT.

Both read and write operations may be performed on this RAM in order to check and/or alter its contents. Since no access to the UUT is made during read and write operations in this address space, no drivability errors will occur.

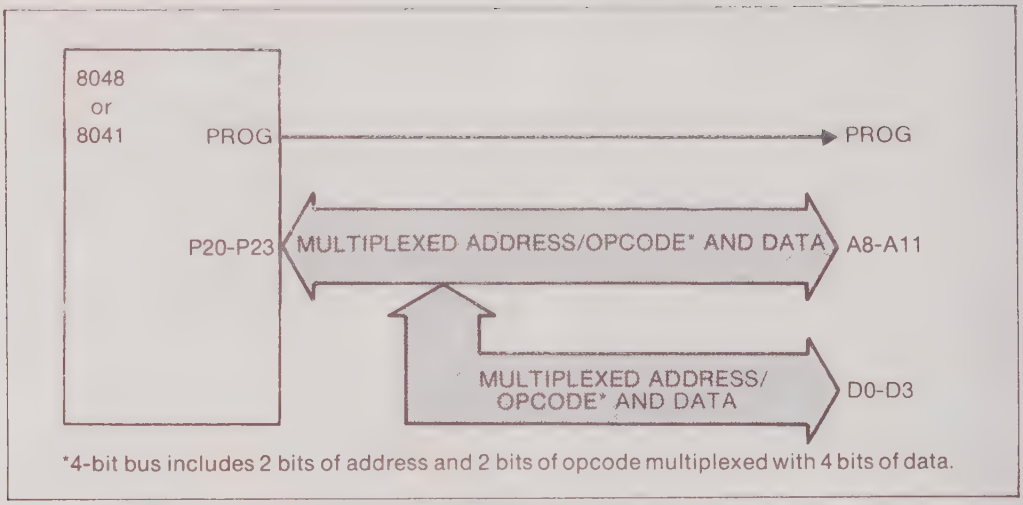

Figure 4-5. Access to Expansion Bus-I/O Ports P4-P7 (Addresses 2004-2007)

4-17. Configuring the T0 line (8048 Family Only)

The T0 line of the 8048 may be configured to be either a testable (through software) input or a clock output. Writing 01 to address 4000 sets the T0 line as a clock output. The T0 line remains a clock output until 00 is written to address 4000 or a reset occurs, in which case the line becomes the testable input.

The function of the T0 line can be checked at any time by performing a read operation at address 4000. If the data read is 01, the line is configured as a clock output. If the data read is 00, the line is configured as an input.

4-18. QUICK LOOPING READ AND WRITE FUNCTIONS

There are two troubleshooting functions that are unique to the 8048/8041 pod: the Quick Looping read and write functions. The repetition rate of the Quick Looping read and write functions is considerably faster than the repetition rate of the ordinary troubleshooter Looping function that is selected by pressing the LOOP key. Because of the increased repetition rate, the Quick Looping functions are particularly useful for enhanced viewing of signal traces on an oscillscope that is synchronized to the TRIGGER OUTPUT pulse (available on the rear panel of the troubleshooter).

Unlike the ordinary troubleshooter Looping function, the software routines that control the Quick Looping functions reside in the pod and not the troubleshooter. The operator selects these functions by accessing the special addresses listed in Table 4-3. For example, a read operation at address 10F00 causes the pod to perform the Quick Looping read operations at address 0F00 (available in the 8048 mode only).

It should be noted that the diagnostics performed by the pod during the execution of the Quick Looping read or write operations are less rigorous than the diagnostics performed during the execution of the ordinary Looping function. The pod reports to the troubleshooter any UUT system errors detected during the first iteration only. Subsequent UUT system errors are not reported.

If both error reporting and the Quick Looping functions are desired, you may apply the ordinary troubleshooter Looping function to the Quick Looping read or write, such as *READ @12000 LOOP*. The troubleshooter will command read operations at address 2000 at the normal looping speed with full error reporting. For every ordinary read operation, the pod will interject a few Quick Looping read operations (with no error reporting) which will enhance oscilloscope viewing.

Table 4-3. Special Addresses for Quick Looping Read and Write Functions

SPECIAL ADDRESS	DESCRIPTION OF USE
10000 to 10FFF*	A read in this address space causes a Quick Looping read in the address space 0000 to 0FFF (8048 mode only).
11100 to 111FF*	A read or write in this address space causes a Quick Looping read or write in the address space 1100 to 11FF (8048 mode only).
12000 to 12002 12004 to 12007	A read or write at these addresses causes a Quick Looping read or write at addresses 2000 to 2002 or 2004 to 2007.
*8048 mode only	

CAUTION

To prevent possible damage to the probe or the UUT, do not use the probe to generate stimulus pulses while a Quick Looping function is being performed if the UUT crystal or clock frequency is less than 1 MHz.

The reason for the preceeding caution is that the combination of the high repetition rate of a Quick Looping function and a slow UUT clock (below 1 MHz) greatly increases the duty cycle of the probe. If the duty cycle is excessively high, the probe stimulus pulses can cause damage to the probe or the UUT. Note that the response capability of the probe, such as logic level reading with the Read Probe operation, is unaffected by high duty cycles.

4-19. CHARACTERISTICS OF THE LEARN OPERATION

The Learn operation of the troubleshooter is designed to operate on bus-oriented systems employing RAM, ROM, and I/O that is external to the microprocessor. While the Learn operation of the troubleshooter may be used with the 8048 and 8041 families of microcomputers, the results are not the same as those achieved with UUTs employing microprocessors.

The Learn operation reports internal RAM (which includes RAM, working registers and stack) in the address space of 1000 to 10FF. The internal RAM is that of the 8048-family microcomputer installed in the socket on the pod, and the amount of internal RAM reported depends upon the type of microcomputer installed in this socket. Microcomputers of the 8035, 8048, and 8748 type contain 64 bytes of RAM, while the 8039, 8049, and 8749 have 128 bytes, and the 8040 and 8050 have 256 bytes. If the Learn operation does not report the expected quantity of RAM, the microcomputer that the operator installed in the pod may be defective.

The Learn operation reports program ROM external to the microcomputer. Internal microcomputer ROM is not accessible and is not reported.

I/O addresses reported by the Learn operation are those addresses which contain read/writable bits, but do not otherwise qualify as RAM. I/O is always reported at location 2000 (bus port for the 8048 family), location 2001 (Port 1), and location 2002 (Port 2). However, the bits reported are those used as outputs. Input lines of the ports may not be reported as I/O. The Learn operation may also report I/O as the expander I/O ports, Port 4 through 7 (addresses 2004 - 2007).

NOTE

If I/O ports cause the Learn operation to stop because of drivability errors on input lines, the reporting of drivability errors may be disabled in the troubleshooter Setup operation by setting the SET-TRAP ADDR ERRORS and/or the *SET-TRAP DATA ERRORS* messages to *NO.* However, if driveability error reporting is disabled to allow the Learn operation to be performed, be sure to enable the error reporting when performing operations other than Learn.

In order for the Learn operation to be properly performed, and in order to provide the greatest possible protection to the UUT circuits, operations at the address 2003 have been implemented such that accesses made to that address cause the bus to revert to a high impedance state. Reads and writes to address 2003 have no effect other than to cause a tristate condition on the bus. This prevents the potentially hazardous possibility of the bus remaining latched and driven following a Learn operation. This feature is handled automatically by the pod and does not require any action by the operator.

4-20. CHARACTERISTICS OF BUS TEST

During Bus Test the troubleshooter assumes that the UUT is a bus-oriented system and comprehensively tests address (8048 family only), data, and control lines for any drivability problems. If the T0 line (8048 family only) is designated as a clock output, it is also tested for drivability. For the 8048 family of devices, Bus Test fully tests the T0 and ALE lines, while other troubleshooter operations test only that ALE is drivable low and T0 (if enabled) is drivable high. For the 8041 family, Bus Test fully tests the SYNC line, while other operations only test that SYNC is drivable low.

If no address is entered for the Bus Test, the pod defaults the test to address 1100 for the 8048 family, and 2000 for the 8041 family to test the data lines, DB0 - DB7. To perform a Bus Test on the lines of I/O Port 1, it is necessary to place the troubleshooter in the Setup mode and enter the address 2001 in response to the message *SET-BUS TEST @ xxxx-CHANGE? (xxxx* is the Bus Test default address). To perform a Bus Test on the lines of I/O Port 2, enter the address 2002 in response to the troubleshooter message *SET-BUS TEST @ xxxx-CHANGE?* A Bus Test to Addresses other than 1100 - 11FF or 2000 - 2002 is not meaningful.

The Bus Test tests the lines for stuck high, stuck low, and tied together conditions. Those I/O lines used as input are reported as having drivability errors, while those used as outputs are fully testable.

4-21. CHARACTERISTICS OF RUN UUT

4-22. Run UUT Addresses for the 8048 Family

The Run UUT operation (described in the troubleshooter operator manual) may be initiated within two different and distinct address spaces. Addresses in the range of 0000 through 0FFF specify locations in either the internal ROM of the microcomputer installed in the pod, or in external program memory of the UUT. Which memory is accessed depends on the address specified and on the state of the EA (external address) input to the microcomputer.

Addresses in the range of 3000 through 30FF access 256 bytes of executable RAM contained within the pod. This RAM may be used to create user-generated test routines. Refer to the Section titled Test Routines in Pod RAM.

4-23. Run UUT Addresses for the 8041 Family

The Run UUT operation (described in the troubleshooter operator manual) may be initiated within the address range of 3000 through 30FF. Addresses in this range access

256 bytes of executable RAM contained within the pod. This RAM may be used to create user-generated test routines in order to exercise the UUT. For programming details, refer to Test Routines in Pod RAM.

NOTE

It is not possible to perform Run UUT from the ROM or EPROM of an 8041 since the pod only operates with an 8048 family microcomputer.

4-24. Test Routines in Pod RAM

There are 256 bytes of RAM memory provided in the pod for operator-supplied test routines that may be performed in the Run UUT mode. The address range of this RAM memory is 3000 - 30FF. Test routines may be written to or read from these locations by performing read or write operations with the troubleshooter. This memory is executable by the microcomputer device (of the 8048 family) that is installed in the pod microcomputer socket. If the particular device being used incorporates instructions other than standard Intel instructions, the extra instructions may be used.

To the executing microcomputer, the RAM appears as program memory in the address range of *X*00 - *X*FF (*X* = any hex digit). The upper four address bits are undecoded; therefore, if address 0FF is exceeded, the memory wraps around onto higher addresses.

When executing the pod RAM, the pod behaves much like a normal 8048 executing its internal program memory. However, there are two important differences that are described as follows:

1. DB0 - DB7 may not be used as an I/O port. Since the bus is used internally to fetch program data, it is not available as an I/O port. The following instructions should not be executed because they would cause unpredictable results:

```
INS     A,BUS
OUTL    BUS,A
ANL     BUS,#DATA
ORL     BUS,#DATA
```

2. DB0 - DB7 and P20 - P23 output the opcode fetch address on each instruction. Although the address is output, the $\overline{\text{PSEN}}$ control line is suppressed so that memory in the UUT will not be enabled. This allows the operator to assert the $\overline{\text{SS}}$ input and follow instruction execution one step at a time. This also means that P20 - P23 may not be used as static I/O ports without the addition of external circuitry.

When operated in the 8041 mode, Port 1, T0, T1, $\overline{\text{Reset}}$, $\overline{\text{SS}}$, and SYNC operate identically to an actual 8041. The data, status, and control registers are not implemented, however, and the bus DB0 - DB7 is unused except for the address information which is output as described above. Port 2 also outputs address information as described above.

The following test program example toggles the Port line P10 whenever T1 is found to have a high input (this example may be used with either the 8048 or the 8041).

ADDRESS	DATA	OPCODE	COMMENT
3000	46	JNT1 00H	Wait for T1 = 1
3001	00		
3002	89	ORL P1,#01H	Toggle P10 high
3003	01		
3004	99	ANL P1,#FEH	Toggle P10 low
3005	FE		
3006	04	JMP 00H	Repeat from beginning
3007	00		

4-25. Run UUT Reset Operations

Operation of the troubleshooter in the Run UUT mode begins by resetting the UUT microcomputer (installed in the pod by the operator). The program counter is then loaded with the address specified by the Run UUT command and operation begins at that address. When the Run UUT mode is terminated (by selecting another function on the troubleshooter) the UUT microcomputer is again reset.

4-26. UNPLANNED RESET OPERATIONS

The UUT microcomputer installed in the pod is not normally reset during troubleshooter operations. Reset normally occurs only upon power-up, upon entering the Run UUT mode, or upon exiting the Run UUT mode. The only other time the microcomputer is reset is if it loses control. If this happens, an intermittent or noisy clock source is indicated, or possibly static discharge to the UUT or pod.

4-27. ACTIVE ALE AND T0 SIGNALS (8048 Family Only)

During all UUT testing, and as long as the UUT power supply is operable, the ALE signal is continuously present. This signal is provided to accommodate those UUTs which depend on ALE in order to remain active. The T0 clock output also remains active during all testing provided that it has been previously configured as an output (described in the section titled Configuring the T0 Line).

There is, however, a time when these outputs are suspended for a period of 2 milliseconds or six instruction cycles, whichever is longer. This occurs whenever the UUT microcomputer installed in the pod is reset, such as when the Run UUT mode is entered or exited. During normal testing, this lack of ALE and T0 signals is of no consequence.

NOTE

The generation of the ALE and T0 output signals is suspended whenever the UUT power level falls to an unsafe level. This feature protects sensitive devices within the UUT which may otherwise be damaged by these signals.

4-28. ACTIVE SYNC SIGNAL (8041 Family Only)

During all UUT testing, and as long as the UUT power supply is operable, the SYNC signal is continuously present. This signal is provided to accommodate those UUTs which depend on SYNC in order to remain active. There is however, a time when the SYNC signal is suspended for a period of 2 milliseconds or six instruction cycles, whichever is longer. This occurs whenever the microcomputer installed in the pod by the operator is reset, such as when the Run UUT mode is entered or exited. During normal testing, this lack of SYNC signal is no consequence.

NOTE

The generation of the SYNC output signal is suspended whenever the UUT power level falls to an unsafe level. This feature protects sensitive devices within the UUT which may otherwise be damaged by this signal.

4-29. PROBE SYNCHRONIZATION MODES

Two synchronization modes are provided by the pod, address sync and data sync. The modes synchronize the troubleshooter probe operation to internal microcomputer events. When enabled, the sync output is active low once during each UUT access. The leading edge of the sync pulse begins at a time slightly prior to the event of interest so that the probe may be activated during the period of interest. The trailing edge of the sync pulse occurs at the moment when address or data is valid. If a probe is being used to capture data, then data should be sampled on the trailing (rising) edge of the sync pulse.

Address sync is generated by gating an inverted version of the ALE signal to the sync output. Data sync may originate from several signal sources: $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, PROG, or UUTON. The source of the data sync signal depends on the type of access in progress. If any other sync mode other than address or data is specified, the sync output of the pod is disabled.

If the pod is being operated in the 8041 mode, the sync pulse behaves as described in the previous paragraphs except that address sync is generated from the 8041 SYNC signal. Although there is no address information to synchronize to, it is common for UUTs to use the SYNC signal to drive a large variety of circuits. By having a mode available by which to synchronize to this signal many UUT operations may be tested and verified.

4-30. CMOS DEVICES AND SLOW CLOCKS

If the microcomputer of the UUT is of the CMOS type and the UUT clock is slow, it may be necessary to change the pod timeout parameter during troubleshooter Setup (the Setup message is *SET-TIMEOUT 200-CHANGE?).* The power-on default value of 200 performs adequately with UUT clocks down to approximately 350 kHz. The maximum timeout parameter of 60000 allows the pod to operate with UUT clocks as slow as 600 Hz. Clock frequencies lower than 600 Hz will cause the troubleshooter to timeout with tests incomplete.

4-31. MARGINAL UUT PROBLEMS

4-32. Introduction

The pod is designed to approximate, as closely as possible, the actual characteristics of the microcomputer it replaces in the UUT. However, the pod does differ in some respects. In general, these differences tend to make marginal UUT problems more visible. A UUT may operate with the actual microcomputer installed, but exhibit errors with the pod plugged in. Since the pod differences tend to make marginal UUT problems more obvious, the UUT is easier to troubleshoot. Various UUT and pod operating conditions that may reveal marginal problems are described in the paragraphs which follow.

4-33. UUT Operating Speed and Memory Access

Some UUTs are designed to operate at speeds which approach the time limits for memory access. The pod contributes a slight time delay which causes memory access problems to become apparent.

4-34. UUT Noise Levels

As long as UUT noise level is low enough, normal operation is unaffected. Removing the UUT from its chassis or case may disturb the integrity of the shielding to the point where intolerable noise could exist. The pod may introduce additional noise. In general,

marginal noise problems will actually be made worse (and easier to troubleshoot) through use of the pod and troubleshooter.

4-35. Bus Loading

The pod loads the UUT slightly more than the UUT microcomputer. The pod also presents more capacitance than the microcomputer. These effects tend to make any bus drive problems more obvious.

4-36. Clock Loading

The pod has a clock oscillator which replaces the UUT microcomputer oscillator. The pod clock oscillator is designed to be less sensitive to capacitive loading than the UUT microcomputer oscillator. However, if the UUT has a clock source other than a crystal, it will experience greater than normal loading due to the capacitance of the pod and its cable. While this loading will rarely have any effect on clock operation, it may make marginal clock sources easier to detect.

4-37. POD DRIVE CAPABILITY

As a driving source on the UUT bus, the pod provides equal to or better than normal 8048/8041 current drive capability. Lines P10 - P17 and P24 - P27 have approximately 100-ohm of series resistance (due to the protection network) between the microcomputer and the UUT. In the Run UUT mode, lines P20 - P23 and T0 have approximately 200 ohms series resistance (100 ohms due to the protection network and 100 ohms due to an analog switch) between the microcomputer and the UUT. All pod inputs and outputs (except the clock and $\overline{\text{Reset}}$) are TTL-compatible.

4-38. POWER FAILURE DETECTION LIMITS

A power sensing circuit within the pod sends a power fail message to the troubleshooter whenever the +5V power supply in the UUT drops below or increases above certain limits. The power failure detection limits are listed in the specifications table in Section 1.

Section 5
Theory of Operation

5-1. INTRODUCTION

The theory of operation of the pod is described on two levels. The first level is an overall functional description which describes the major sections of the pod and how they relate to each other and to the UUT and the troubleshooter. The second level is a detailed block diagram of each pod section. The descriptions are supported by block diagrams and timing diagrams in this section, and by complete instrument schematics in Section 8 of this manual.

5-2. GENERAL POD OPERATION

The pod may be divided into five major areas:

- Master Processor Section
- Slave Processor Section
- UUT Interface Section
- Timing and Control Section
- UUT Power Sensing

Each section is described in the following paragraphs.

5-3. Master Processor Section

The Master Processor Section, shown in Figure 5-1, is made up of a processor, RAM, ROM, an I/O interface to the troubleshooter, and bus buffers (the "processor" is actually a microcomputer, but during this discussion it is referred to as a processor because of its function in the Master Processor Section). These elements comprise a small computer system which receives troubleshooter commands and directs all pod operations during execution.

The RAM is shared with the Slave Processor Section. Instructions to be executed by the slave processor (which, like the master processor, is a microcomputer functioning as a processor) are moved to the RAM and saved there until the slave processor is commanded to execute those instructions. Results of read operations are returned by the slave processor by placing them in the RAM. The master processor may then get the result and further process it.

5-4. Slave Processor Section

The Slave Processor Section, shown in Figure 5-1, consists of a processor (which is the microcomputer that is installed by the operator in the screw-actuated microcomputer

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5-4. Slave Processor Section

The Slave Processor Section, shown in Figure 5-1, consists of a processor (which is the microcomputer that is installed by the operator in the screw-actuated microcomputer

socket on the pod), RAM, and bus buffers. The processor inserted in the socket is that which performs actual accesses to the UUT. If the UUT is based on one of the 8048 family microcomputers, this processor may be the UUT microcomputer that was removed from the UUT prior to testing. An 8048 family UUT microcomputer may contain programs in its internal ROM that are needed to operate in the Run UUT mode. If the processor is not an 8048 family UUT microcomputer, it must be one of the 8048 family microcomputers, even if the UUT is based on one of the 8041 family microcomputers.

Although the pod operates with both 8048-based and 8041-based UUTs, the pod will not operate with an 8041 family microcomputer installed. This is because the 8041 is a true single-chip microcomputer and has no facility to allow access to external program or data memory and cannot execute instructions from an external program source. Therefore, it is not possible to use an 8041 family microcomputer as the slave processor since the slave processor must be able to fetch and execute instructions from the pod RAM that is shared with the master processor.

The slave processor normally operates in a single-step mode during most troubleshooter operations. Under control of the master processor, instructions are executed from the shared RAM. The bus buffers are controlled such that only the master or the slave may access the shared RAM at one moment.

Much of the internal timing of the pod depends on the the slave processor's T0 clock. This clock operates internal to the pod at all times. If the UUT requires this clock signal to maintain dynamic RAM, display refresh, etc., it may be enabled to the UUT through the T0 configuration address (4000 hex).

5-5. UUT Interface Section

The UUT Interface Section, shown in Figure 5-1, includes the following elements:

- Data and address buffers
- Protection circuits for signal lines
- Logic level detection circuits for data, address, status, and control lines
- Clock oscillator circuit

The data and address buffers are enabled to connect the slave processor to the UUT, or disabled to isolate the slave processor from the UUT. Control of the buffers is maintained by the Timing Section.

Each line to the UUT contains a protection circuit. A protection circuit consists of a 100-ohm resistor in series with a pair of clipping diodes. This circuit prevents over voltage conditions from damaging pod components.

Each line to the UUT also contains a detection circuit. A detection circuit consists of a latch connected to the UUT side of the 100-ohm protection resistor. The latch senses the level at the UUT side of the protection circuit, and at the conclusion of each UUT operation, stores the level of the UUT line. Each latch is then individually addressed and read by the Master Processor Section. Their contents are then compared with the desired results as a means of detecting UUT bus faults.

Also in the UUT Interface Section is an oscillator circuit that takes the place of the built-in oscillator of the slave processor. This oscillator is especially designed to be less sensitive to the capacitive loading present in the UUT cable than are typical slave processor

oscillators. To the user and to the UUT, this oscillator should appear and behave identically to the usual built-in processor oscillator.

5-6. Timing and Control Section

The primary purpose of the Timing and Control Section is to control the buffers to the shared RAM and UUT, and to control the single stepping of the slave processor. The Timing and Control Section is also responsible for triggering the level sensing latches.

The Timing and Control Section of the pod, shown in Figure 5-1, consists of an interval counter, I/O ports and several control and timing circuits. These circuits are described more fully in the description of the detailed block diagram.

Since the slave processor is essentially halted most of the time, and since many UUTs depend on the presence of ALE (or SYNC) as a clock source, there is a special circuit incorporated in the pod which generates a continuous ALE signal. This signal is fully synchronized with all slave processor actions.

In preparation for a UUT access, the Master Processor Section loads a series of instructions to the shared RAM. The master processor then causes the timing and control ciruits to single-step the slave processor through several instructions up to the point that the next instruction is the one which is desired to access the UUT.

At this point the Timing and Control Section is setup to cause the second cycle of the next instruction to access the UUT. During the execution of that instruction a state counter is used to control buffers and trigger latches at the appropriate times.

The slave processor is then stepped once and the UUT is accessed. Following the step the control and timing circuits revert to their previous state. The slave processor may then be stepped several more times to cause the result, if any, to be returned to the shared RAM.

The Master Processor section then reads the results from RAM and the level sensing latches. The data is processed and returned to the troubleshooter.

When the Run UUT mode is selected, the Master Processor Section causes the Timing and Control Section to switch on all the buffers to the UUT. The slave processor is then allowed to free-run.

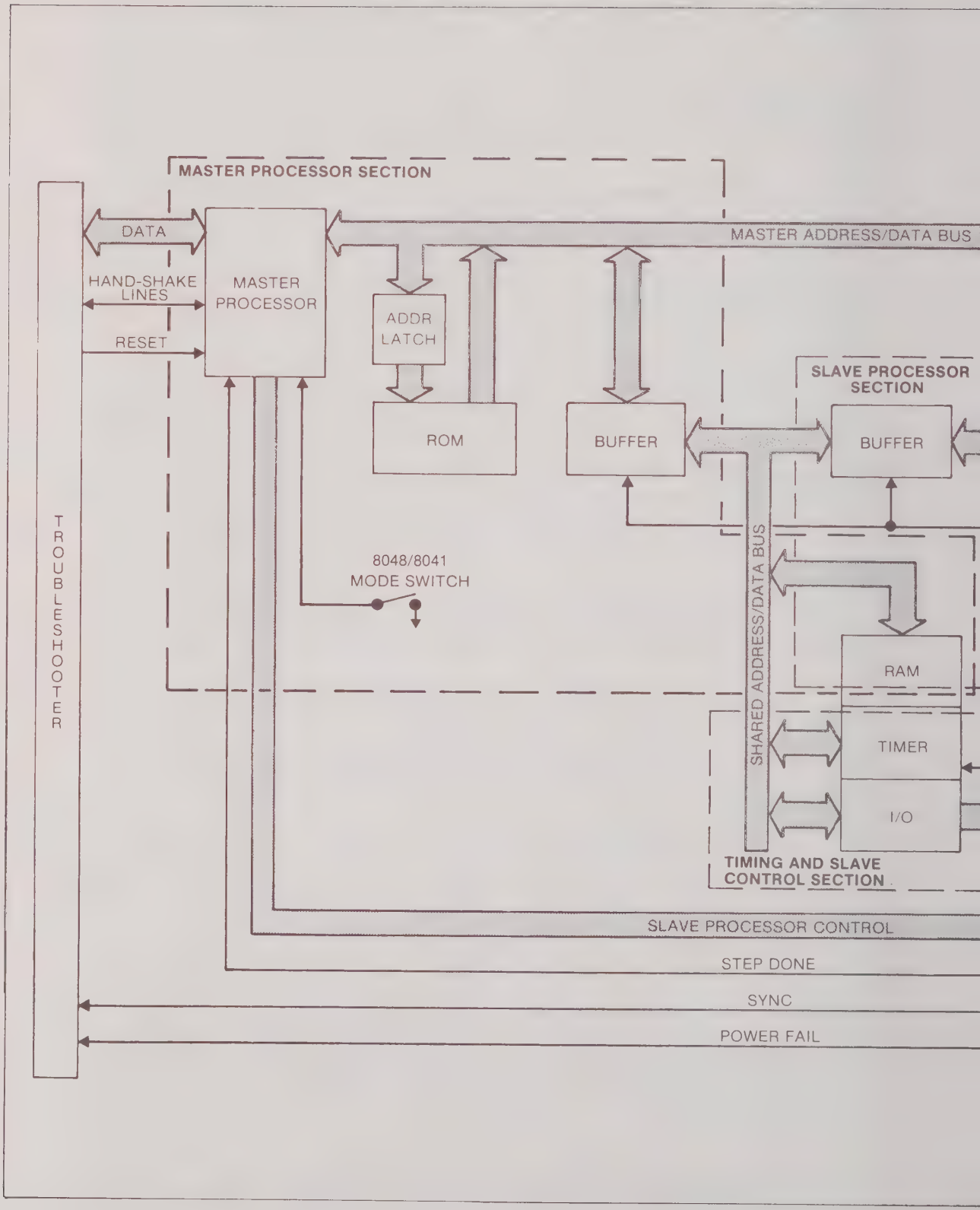
5-7. UUT Power Sensing

The power sensing circuit shown in Figure 5-1 constantly monitors the UUT power supply. This circuit produces an output to the troubleshooter in the event UUT power drops below 4.5V or rises above 5.5V.

Also, anytime the UUT power supply drops below about 3.4V, all active pod outputs are disabled or written to their low logic level. This feature has been incorporated to protect UUT circuits from being damaged by pod outputs when the UUT power supply drops below safe operating limits. The troubleshooter will display a UUT power-fail error message, or, if the power-fail messages have been disabled, the troubleshooter will indicate a pod timeout error message. When the proper operating power supplies have been restored to the UUT, the outputs of the pod will return to normal and the troubleshooter will be ready for additional testing.

5-8. DETAILED BLOCK DIAGRAM DESCRIPTION

A detailed block diagram of each major pod section is presented in Figure 5-2. Each section is described in the following paragraphs.


MASTER PROCESSOR SECTION
DATA
HAND-SHAKE LINES
RESET
MASTER PROCESSOR
MASTER ADDRESS/DATA BUS
ADDR LATCH
ROM
BUFFER
SLAVE PROCESSOR SECTION
BUFFER
TROUBLESHOOTER
8048/8041
MODE SWITCH
SHARED ADDRESS/DATA BUS
RAM
TIMER
I/O
TIMING AND SLAVE CONTROL SECTION
SLAVE PROCESSOR CONTROL
STEP DONE
SYNC
POWER FAIL

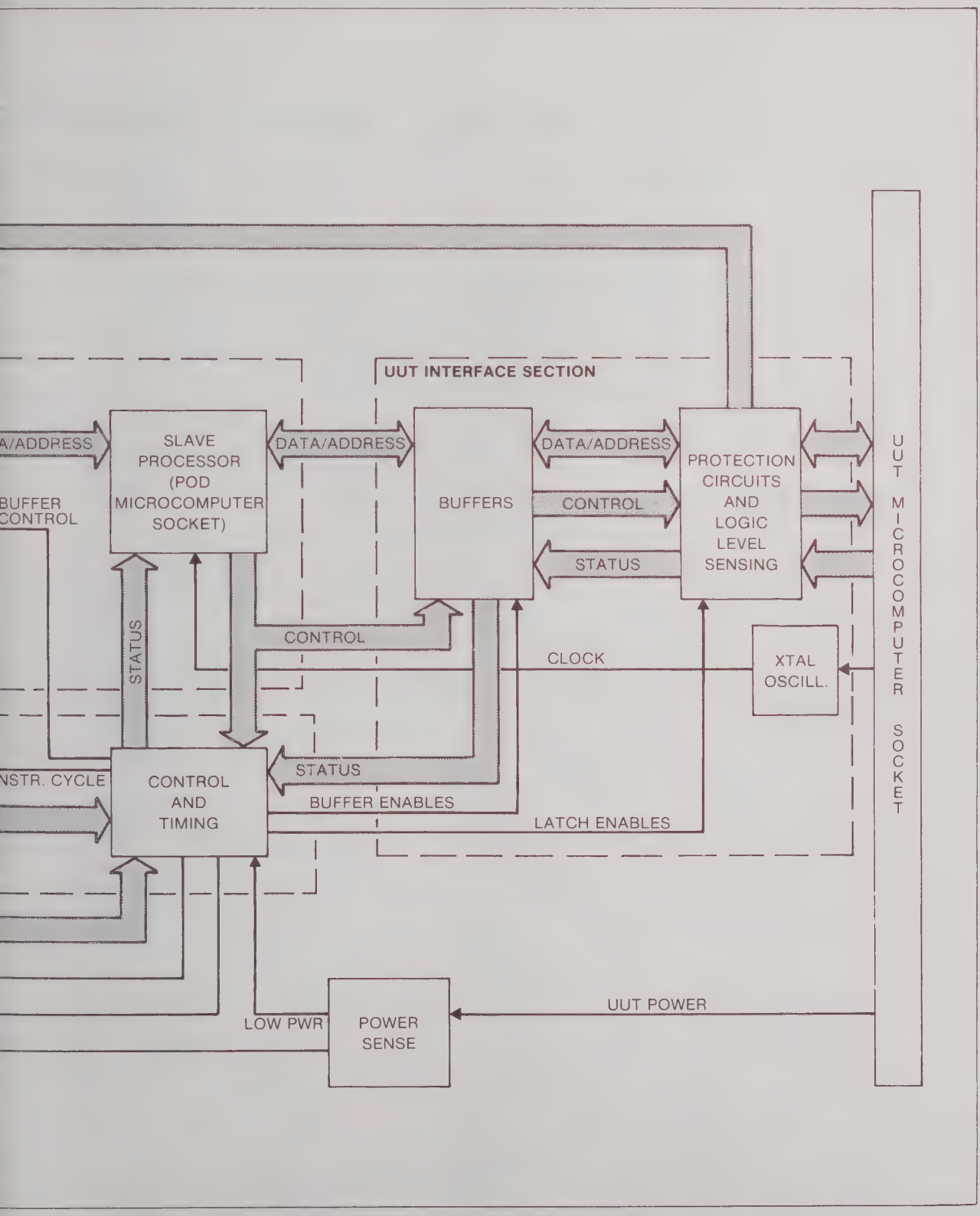
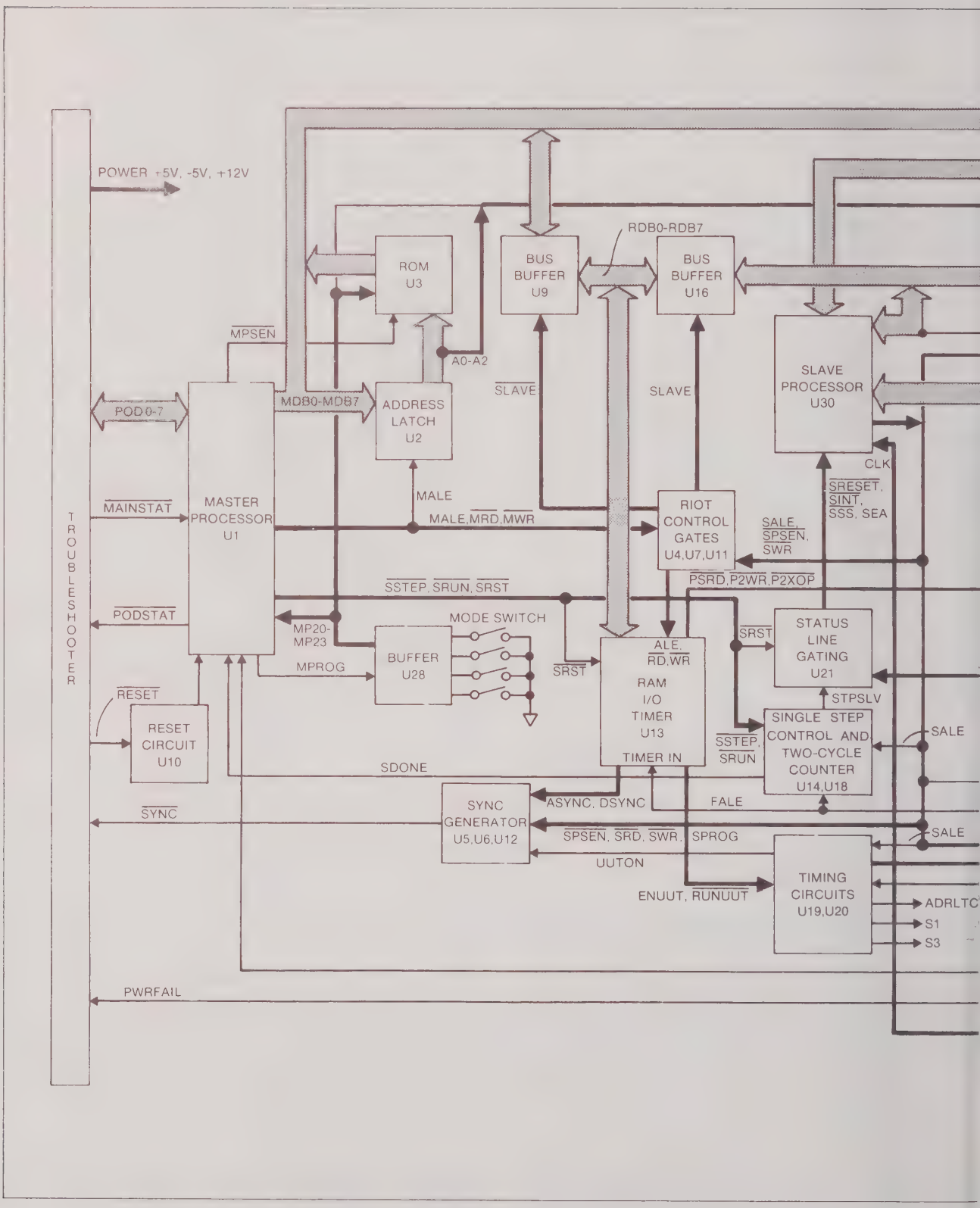


Figure 5-1. 8048 Interface Pod General Block Diagram


TROUBLESHOOTER
POWER +5V, -5V, +12V
ROM U3
BUS BUFFER U9
BUS BUFFER U16
RDB0-RDB7
MPSEN
A0-A2
SLAVE
SLAVE
SLAVE PROCESSOR U30
CLK
SRESET, SINT, SSS, SEA
POD 0-7
MDB0-MDB7
ADDRESS LATCH U2
MAINSTAT
MASTER PROCESSOR U1
MALE
MALE, MRD, MWR
RIOT CONTROL GATES U4,U7,U11
SALE, SPSEN, SWR
PSRD, P2WR, P2XOP
SSTEP, SRUN, SRST
PODSTAT
MP20-MP23
MODE SWITCH
BUFFER U28
MPROG
SRST
ALE, RD, WR
RAM I/O TIMER U13
TIMER IN
SRST
STATUS LINE GATING U21
STPSLV
RESET
RESET CIRCUIT U10
SSTEP, SRUN
SINGLE STEP CONTROL AND TWO-CYCLE COUNTER U14,U18
SALE
SDONE
SYNC
SYNC GENERATOR U5,U6,U12
ASYNC, DSYNC
FALE
SALE
SPSEN, SRD, SWR, SPROG
UUTON
ENUUT, RUNUUT
TIMING CIRCUITS U19,U20
ADRLTC
S1
S3
PWRFAIL

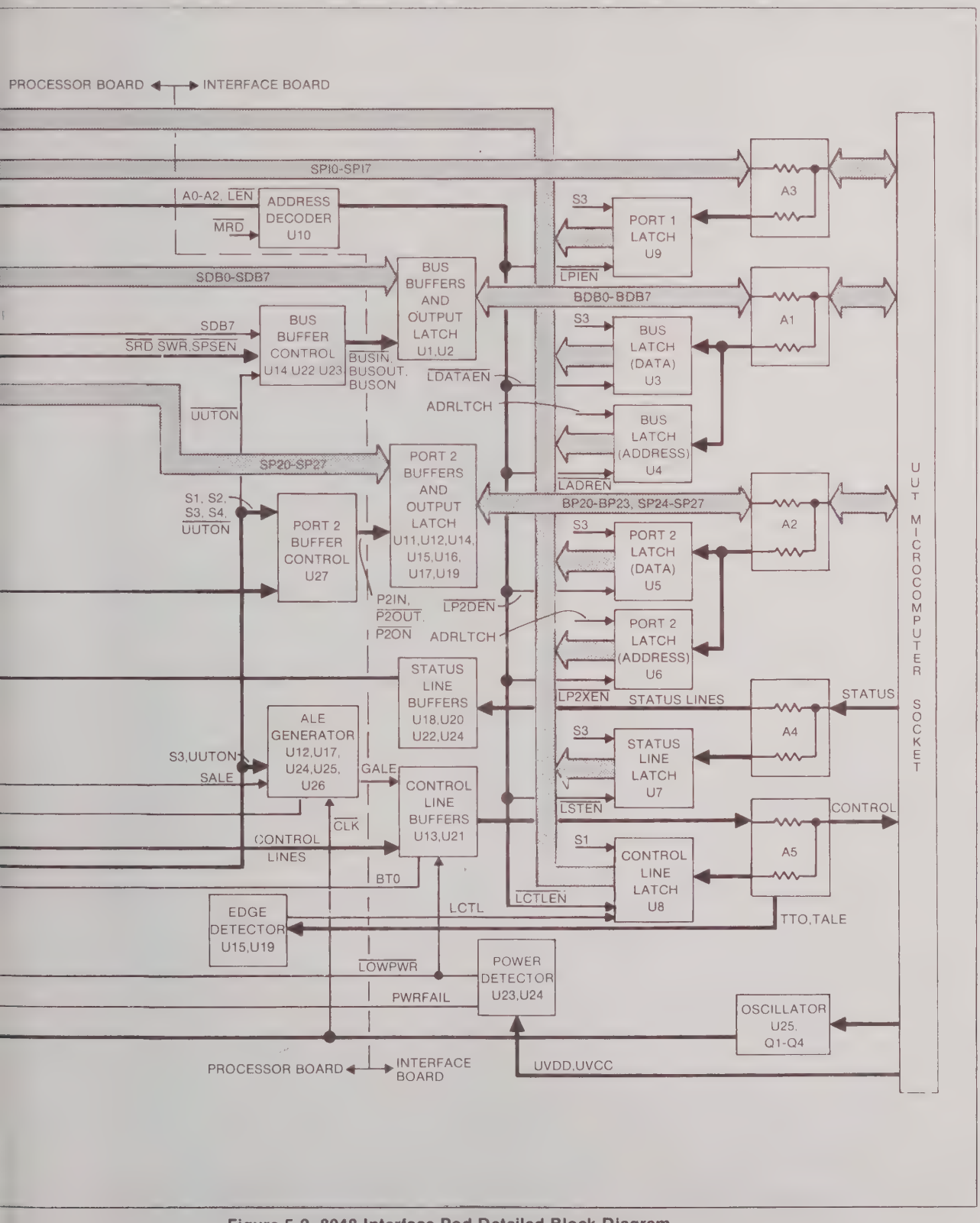


Figure 5-2. 8048 Interface Pod Detailed Block Diagram

5-9. Master Processor Section and Slave Processor Section

The Master Processor Section is made up of the following components:

- Microcomputer, U1
- ROM and ROM address latch, U2 and U3
- RAM (256 bytes x 8 bytes), U13
- I/O ports 1 and 2, U1
- Input port, U28
- Bus buffer, U9
- Reset circuit, U10

The Slave Processor Section is made up of the following components:

- U30, UUT microcomputer (or alternate part), installed in socket J3
- RAM (256 bytes x 8 bytes), U13
- Bus buffer, U16

Pod resets cause the master processor, U1, to be reset through the reset circuitry of U10. This circuit synchronizes asynchronous resets from the troubleshooter with the master processor's state machine so that all resets received will function properly.

The master processor monitors the setting of the mode switches by reading the I/O port at U28. Presently only one bit of data is used to convey mode information.

The master processor section also monitors the handshake line, $\overline{\text{MAINSTAT}}$, on I/O line T0 of the processor, and waits for troubleshooter commands. The troubleshooter places a low on the $\overline{\text{MAINSTAT}}$ line when a command is placed on lines POD0 - POD7. The master processor responds by reading each byte of the troubleshooter command at its I/O port 1 and handshaking with the $\overline{\text{PODSTAT}}$ line on Port 2. As each byte is received, the handshaking lines operate as shown in the upper portion of Figure 5-3 to assure that no data is lost.

Each troubleshooter command causes the microprocessor to execute a corresponding routine contained in ROM U3. This routine, when executed, performs the troubleshooter command by first setting the slave processor's program counter to point to a routine in the shared RAM, U13, which, when executed, will address the UUT. Routines in the shared RAM are loaded by the master processor from the ROM each time the pod is reset.

The routine continues with the performance of various operations in preparation for the addressing of the UUT. Part of the preparation requires writing address and/or data information to the shared RAM. RAM is addressed by addresses on the multiplexed address/data bus of the master processor and by the processor's I/O port 2. During this period, bus buffer U9 is enabled and bus buffer U16 is disabled. The master processor then single-steps the slave processor through several initialization instructions. This single-stepping is accomplished by writing commands to the I/O Port 2 of U1. Each time the slave processor is stepped, the bus buffer U9 is disabled and the bus buffer U16 is enabled, thus allowing the slave processor to fetch instructions from the shared RAM.

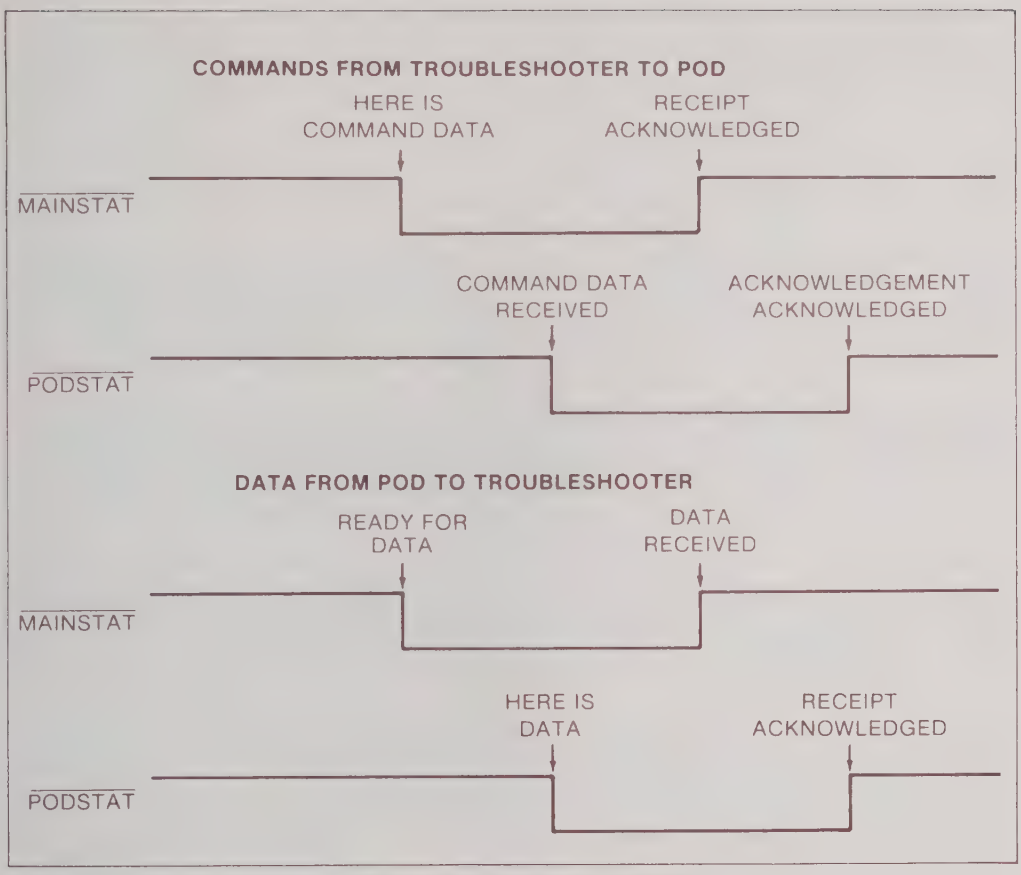


Figure 5-3. Handshake Signals

Next, various control lines on ports A, B, and C of U13 are set up prior to the UUT access. This configures the timing circuitry to allow the second cycle of the next instruction executed by the slave processor to access the UUT. The slave processor is then single-stepped once, and the UUT access is made. Control lines on ports A, B, and C are changed back to their standby state.

The routine is completed with the single-stepping of the slave processor a few more times, with any read results returned. The master processor reads those results from the shared RAM and reports them to the troubleshooter.

5-10. UUT Interface Section

5-11. GENERAL

The UUT Interface Section includes the following components shown in Figure 5-2:

- Bus buffers and output latch, U1, U2
- Port 2 buffers and latch, U11, U12, U14, U15, U16, U17, U19
- Status line buffers, U18, U20, U22, U24
- Control line buffers, U13, U21
- Protection circuits, A1 through A5

- Sensing latches, U3 through U9
- Edge detector, U19
- Oscillator, U25, Q1 through Q4
- Low power detector, U23, U24

5-12. DATA LINES

The data lines are input through an octal buffer, U1. During UUT read operations this buffer is enabled. Note that the bus buffer, U16, may be enabled during an instruction fetch from the shared RAM, U13, but then the input buffer, U1, is enabled during the second cycle of a read operation.

The data (and multiplexed address) lines are output through the three-state octal latch, U2. In the case that the bus is being used as an I/O port in the output mode, data is latched at the output with the output left enabled. If the bus is not used as an I/O port in the output mode, then data is only output momentarily at appropriate times during a UUT access.

All data and low-order addresses passing between the pod and the UUT are fed through a series of protection circuits, with one circuit per line. Each protection circuit consists of a 100 ohm resistor in series with the line, and a pair of clipping diodes. The diodes clip the data line at zero and +5 volts.

The address/data lines are also equipped with logic level detection circuits, with one circuit per line. The detection circuits consist of a series of latches coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The address/data lines are coupled to the inputs of latches U3 (data) and U4 (address) by lines LDB0 - LDB7. The input to each latch is logic high if the line is driven high, and logic low if the line is driven low. The address/data line logic levels are latched by the S3 and ADRLTCH signals from the Control and Timing Section. The ADRLTCH signal causes latch U4 to store the logic levels representing the state of each line when carrying a low-order address. The S3 signal causes latch U3 to store the logic levels representing the state of each line when carrying data.

At the conclusion of a UUT write operation, latches U3 and U4 are addressed by the master processor. Address decoder U10 produces the $\overline{\text{LADREN}}$ and $\overline{\text{LDATAEN}}$ signals to place the contents of the latches sequentially on the data bus. The master processor compares the contents of the addressed latches with the intended write address and data. Any difference between the contents of the latches and the intended data is considered an error.

5-13. PORT 1 AND PORT 2 LINES

In a manner similar to that described for the address/data lines, all of the Port 1 and Port 2 lines are fed through a series of protection circuits equipped with resistors and clipping diodes. The Port 1 lines have no further buffering, but are connected directly to the slave processor through lines SP10 - SP17. Also, the four most significant lines of Port 2, SP24 - SP27, are connected directly to the slave processor without additional buffering.

The lower four Port 2 lines run through protection circuits in the same way as described previously for the upper four lines. The output of these four lines goes through a latch and a series of gates and buffers so that the true function of the lines is accurately duplicated.

U12 is used as an output latch. When data is written high, the output buffers in U17 are strobed on momentarily by the gates, U16. Lines which are written high remain high due to the action of the pull-up resisters in Z3 after the momentary drive ceases. Any lines which are written low remain driven due to U16 and U17.

Lines which have data written high may be used as inputs. NAND gates in U14 are used to strobe the input buffers in U15 on those lines which are used as inputs.

During Run UUT operations, the Port 2 buffers are bypassed by analog switches, U11 and U19. In this mode, the lines are connected directly to the slave processor with a total series resistance (due to the protection circuit and the analog switch) of approximately 200 ohms.

As described for the address data lines, the Port 1 and Port 2 lines are equipped with logic level detection circuits, with one circuit per line. The detection circuits consist of a series of latches coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The Port 1 lines are coupled to the inputs of latch U9 by lines LP10 - LP17. Port 2 lines are connected to latches U5 and U6 by lines LP20 - LP27. The input to each latch is logic high if the line is driven high, and logic low if the line is driven low. The S3 signal from the Timing and Control Section latches the data logic levels on latches U5 and U9. ADRLTCH latches data logic levels on latch U6.

At the conclusion of a UUT operation, latches U5, U6, and U9 are addressed by the master processor. Address decoder produces the $\overline{\text{LP1EN}}$, $\overline{\text{LP2DEN}}$, and $\overline{\text{LP2XEN}}$ signals to place the contents of the latches sequentially on the data bus. The master processor compares the contents of the latches with the intended data or address. Any difference between the contents of the latches and the intended data or address is considered an error.

5-14. CONTROL AND STATUS LINES

The status and control lines are provided with protection circuits, logic level detection circuits, and latches. These circuits operate in a manner similar to those provided with the data and address lines, and described in the previous paragraphs. Control lines $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{PSEN}}$ are buffered by U13. PROG and ALE are buffered by the gates of U21. ALE, which is generated by the Timing and Control Section, is active at all times. The status lines $\overline{\text{SS}}$, $\overline{\text{INT}}$ and EA are buffered by U18. T1 is unbuffered; the line ST1 runs directly to the slave processor.

When the pod is being operated in the 8041 mode, the $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{PSEN}}$ signals are no longer output. The buffers in U13 tri-state these control lines and allow them to be monitored instead as status inputs $\overline{\text{RD}}$, $\overline{\text{WR}}$, and A0.

The T0 line may be configured as an input or a clock output. As a clock output, buffer U13 is enabled which allows the ST0 signal to be output. When performing a Run UUT, U13 is disabled and the analog switch, U19, is enabled. This allows the T0 line to function as an input or output under control of the UUT's or user's programs.

T0 and ALE are connected to a data selector, U15, the output of which is connected to an edge detector, U19. If activity is found on the selected line, the edge detector registers that activity and the result is fed to the control line latch, U8, via the LCTL line. This is necessary since these lines may have activity which occurs more quickly than what may normally be encountered by the latches.

The status lines are connected to the inputs of latches in U7, and the control lines are connected to latches in U8. Status lines are latched by the control signal S3, and the control lines are sampled by the signal S1. At the end of a UUT operation the latches are addressed by the master processor and the address decoder in the same way as the other lines previously described. If latches for the control lines do not contain the expected results, errors are considered to have occurred.

5-15. OSCILLATOR

U25 and transistors Q1 through Q4 comprise an oscillator circuit. This circuit replaces the slave processor's built-in oscillator on pins XTAL1 and XTAL2. The oscillator is designed to perform in the same way as the slave processor's oscillator, with the exception that it is less sensitive to stray capacitive loading. This allows the oscillator to function properly even though the pod is removed several inches from the UUT through the UUT cable. The buffered clock outputs CLK and $\overline{\text{CLK}}$ are connected to the slave processor and to the Timing and Control Section.

5-16. LOW POWER PROTECTION

A low power detection circuit has been incorporated in this pod to protect the UUT in the event that the UUT power supply falls to an unusually low voltage level. The low power detector is made up of the Schmitt trigger circuit of U24. The trigger points of this circuit are nominally 3.4V and 3.6V.

In the event that a low power condition is detected, the control line buffers in U13 and the data bus buffers in U2 change to their high impedance state. ALE, PROG, and the I/O port lines P10 - P17 and P20 - P27 are changed to a low logic level output. During this time, no high logic level outputs are allowed to occur for any length of time that would be damaging to the UUT.

Also, anytime the UUT power supply is not within the normal operating limits of 5V ±10%, the power supply monitor U23 tracks and reports that condition to the troubleshooter through the POWERFAIL signal.

5-17. Control and Timing Section

The Control and Timing Section includes the following components as shown in Figure 5-2:

- Single-step control, U14
- Two-cycle counter, U18
- Bus buffer control, U14, U22, U23
- Port 2 buffer control, U27
- Timing circuits, U19, U20
- ALE generator, U12, U17, U24, U25, U26

The single-step control U14 is used to control the slave processor as the master processor presents instructions to be performed. Each time the slave processor is stepped, one instruction is executed. The two-cycle counter assumes that an instruction is complete when two instruction cycles have been executed. All 8048 instructions are either one or two cycles in length. The single-stepping of the slave processor is illustrated in Figure 5-4 and proceeds as follows:

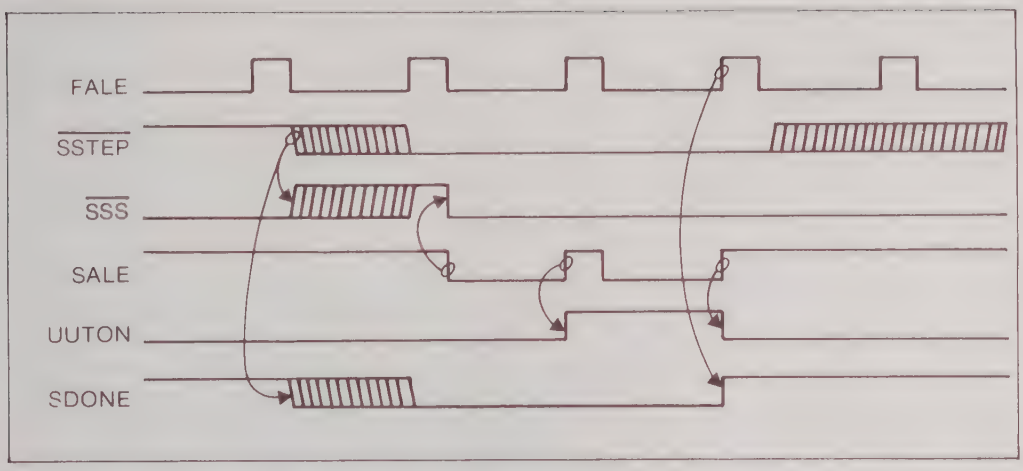


Figure 5-4. Single Step and UUTON Timing

1. The master processor asserts the line $\overline{\text{SSTEP}}$.

2. Flip flop U14 is set by $\overline{\text{SSTEP}}$ and causes $\overline{\text{SSS}}$ to be applied to the slave processor. Flip flops U18 are also reset by this action.

3. As the slave processor begins an instruction fetch from U13, the falling edge of SALE resets flip flop U14 and removes $\overline{\text{SSS}}$ from the slave processor.

4. The first rising edge of SALE clocks flip flop U19 and causes UUTON to be asserted. The UUT access begins at this time.

5. The next rising edge of SALE ends UUTON and the UUT access is complete.

6. FALE is synchronized to SALE and occurs once during each machine cycle. A two-cycle counter consisting of U18, which is reset in Step 2, is clocked on each rising edge of FALE. When two cycles have been counted, SDONE is asserted. This is read by the master processor and the single-step operation is complete.

With the SDONE signal as feedback from the slave processor to the master processor, the two processors are able to synchronize actions even though they might actually be running at extremely different clock frequencies.

The bus buffer control circuit is responsible for controlling inputs, outputs, and the latching of data on the address/data buffers. Flip-flop U14 is used to store the state of the bus port (whether it is being used as a latched output or as an input). U23 is a combinational logic array which implements a complex set of rules necessary for proper operation of the bus buffers. Inputs to this array include control outputs from the slave processor, and control outputs generated by the master processor through an I/O port. When performing in the Run UUT mode, comparators in U22 determine those times when the bus is driven, and affect control of the bus buffers.

Port 2 buffer control is generated by the combinational logic array U27. This affects only the four lower bits of the port; the upper four bits are unbuffered. Inputs to the logic array include control lines generated by the master processor through an I/O port, and from the timing circuits described further below. During Run UUT no buffer control is needed since the buffers are bypassed by the analog switches.

The timing circuits are used to define the window of time used to access the UUT (UUTON), and to generate an instruction cycle state counter. Flip-flop U19 generates the UUTON signal which is used to initiate accesses to the UUT. When enabled, flip-flop U19 creates the UUTON signal for the duration of the second cycle of the current slave processor instruction. Shift register U20 implements the state counter. The shift register is clocked by the slave processor's T0-clock signal. The state counter outputs are used by the buffer control sections described above and by the logic level detection latches as trigger inputs.

The final task of the Control and Timing Section is the generation of the ALE signal. Since many UUTs depend on ALE (or SYNC in the case of the 8041) as a clock source for display refresh, etc., and since the slave processor is halted (which also stops ALE) much of the time, it is necessary to have a special circuit to generate ALE signals between UUT accesses. Shift registers U25 and U26 form the heart of the ALE generation circuit. This circuit is initialized when the slave processor is reset. As soon as the shift registers have a picture of the ALE waveform, the generated ALE signal is available. During each UUT access the real ALE signal is output; between accesses, the generated ALE is output. The circuit is synchronous and glitch free.

5-18. Examples of Signal Timing Relationships

Figure 5-5 provides examples of signal timing relationships for read and write operations at a variety of addresses. Note that some examples pertain only to the 8048 microcomputer family, and some pertain only to the 8041 microcomputer family.

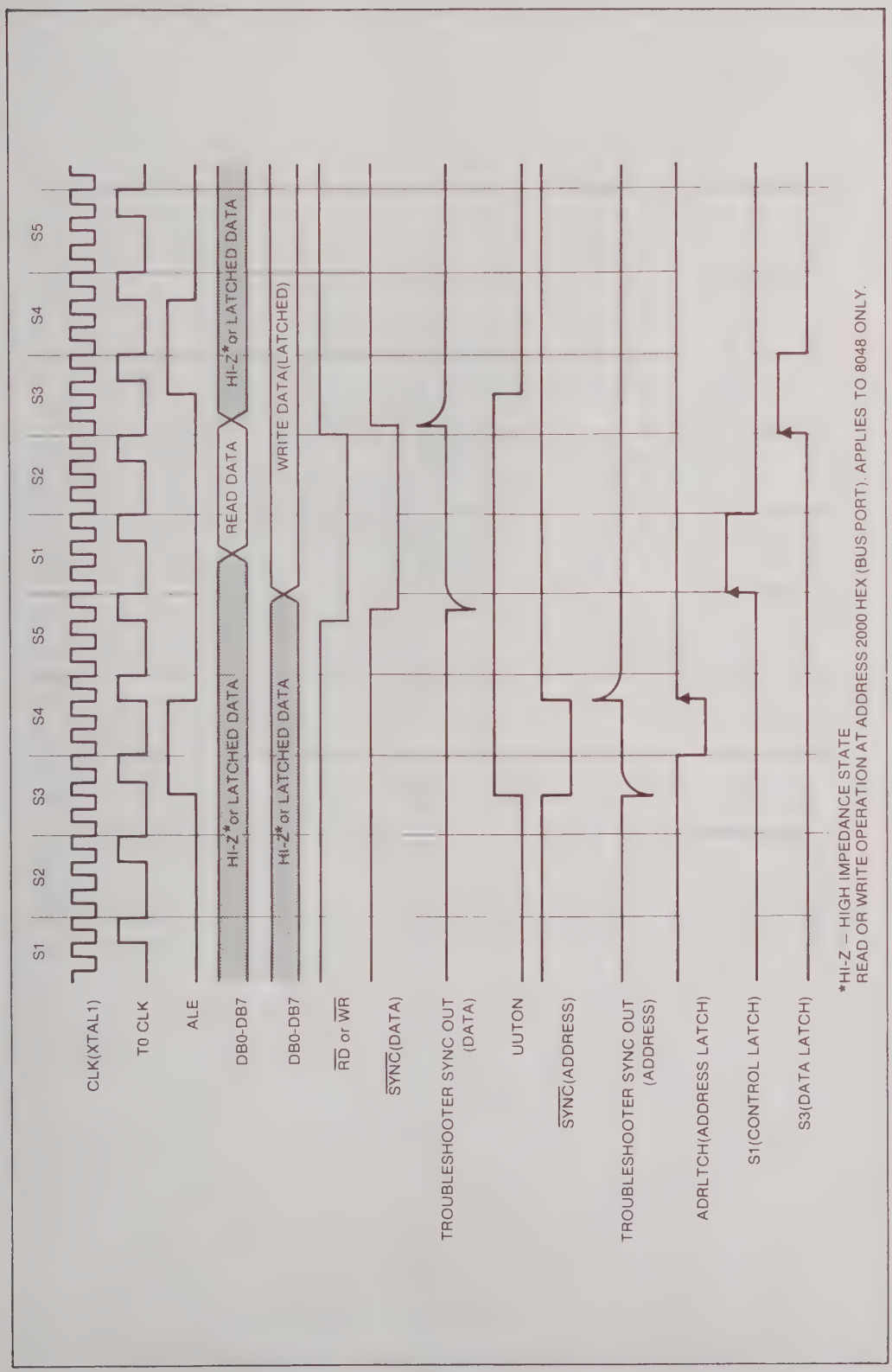


Figure 5-5. Examples of Signal Timing Relationships

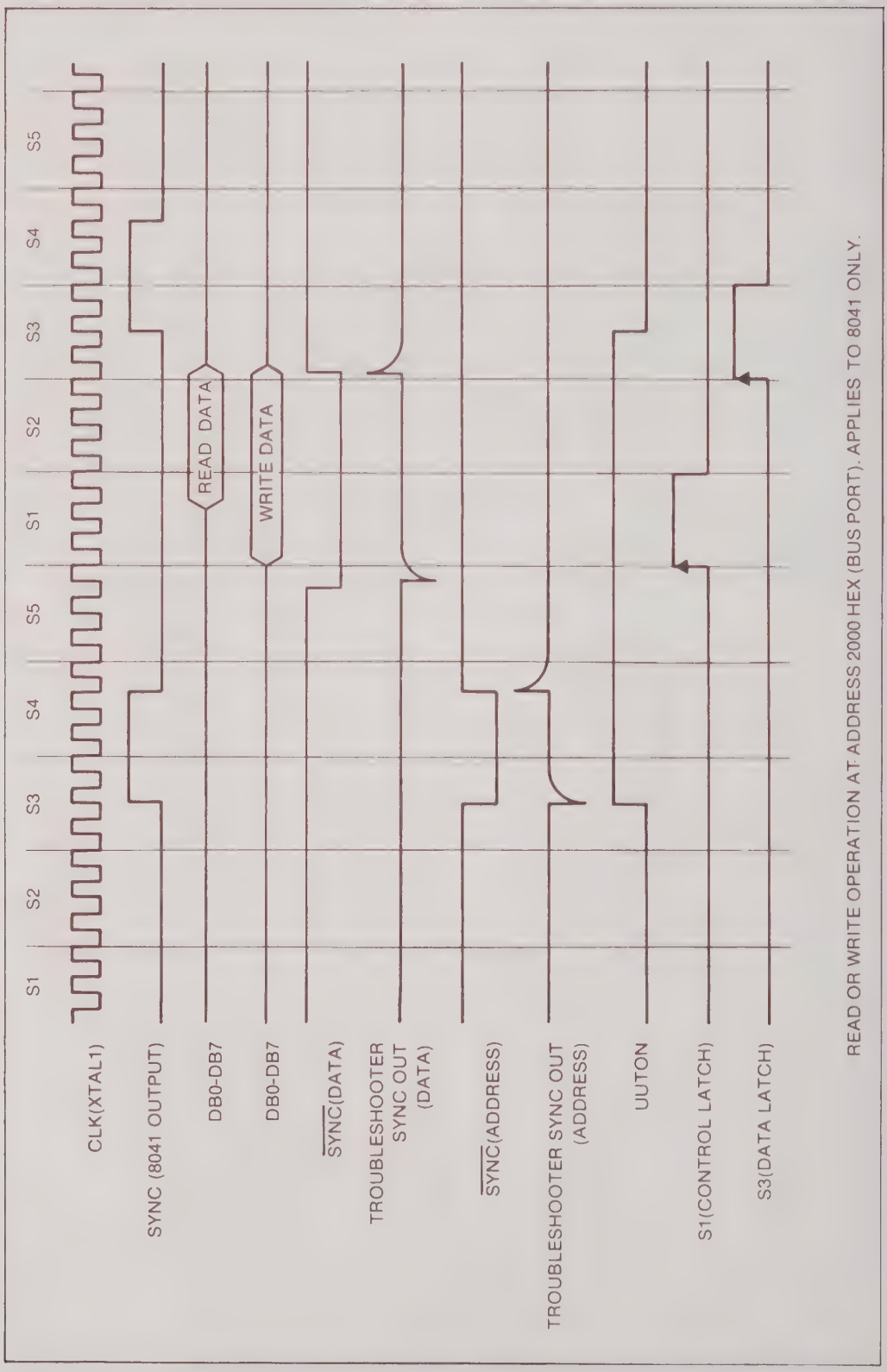


Figure 5-5. Examples of Signal Timing Relationships (cont)

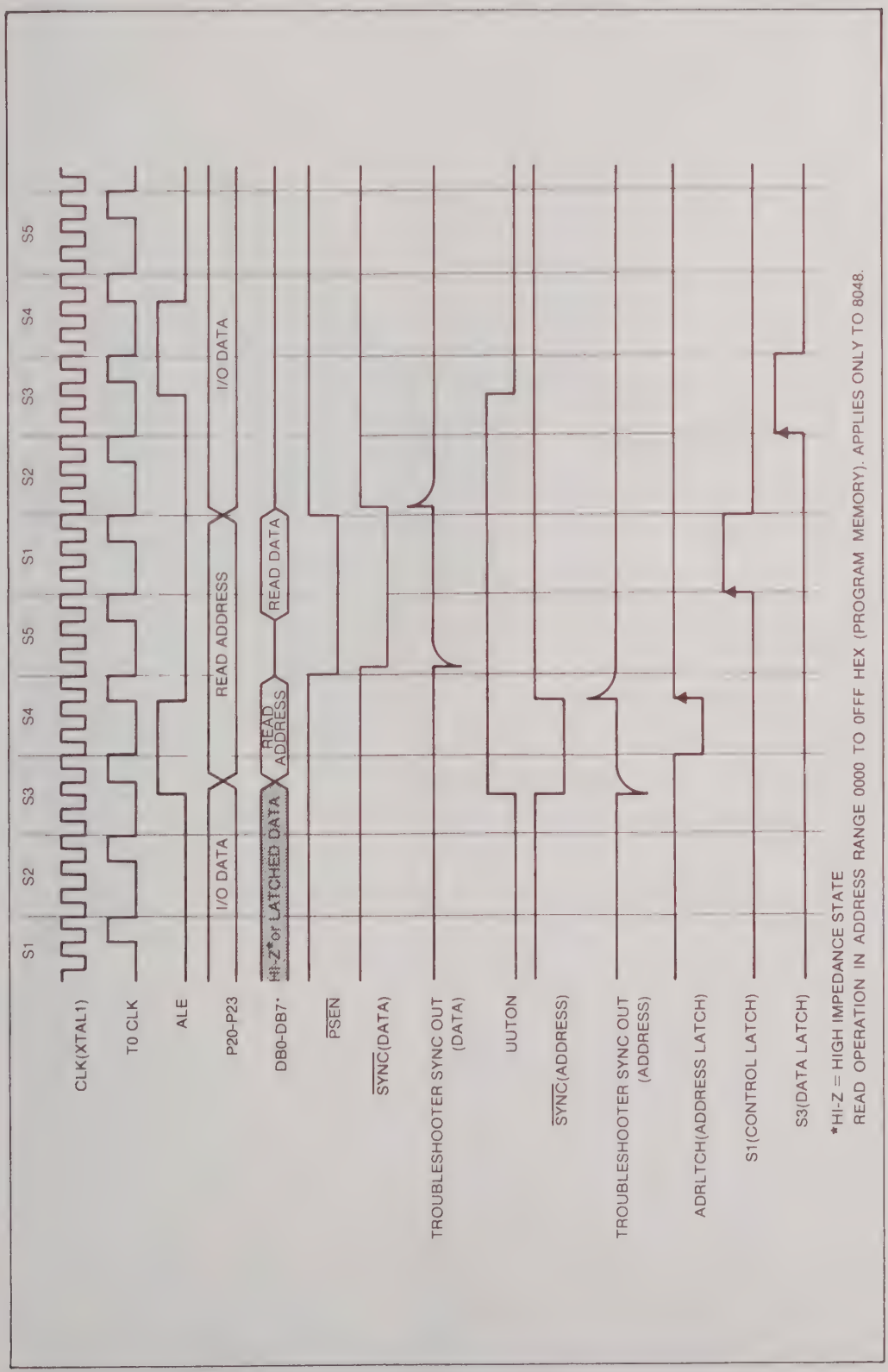


Figure 5-5. Examples of Signal Timing Relationships (cont)

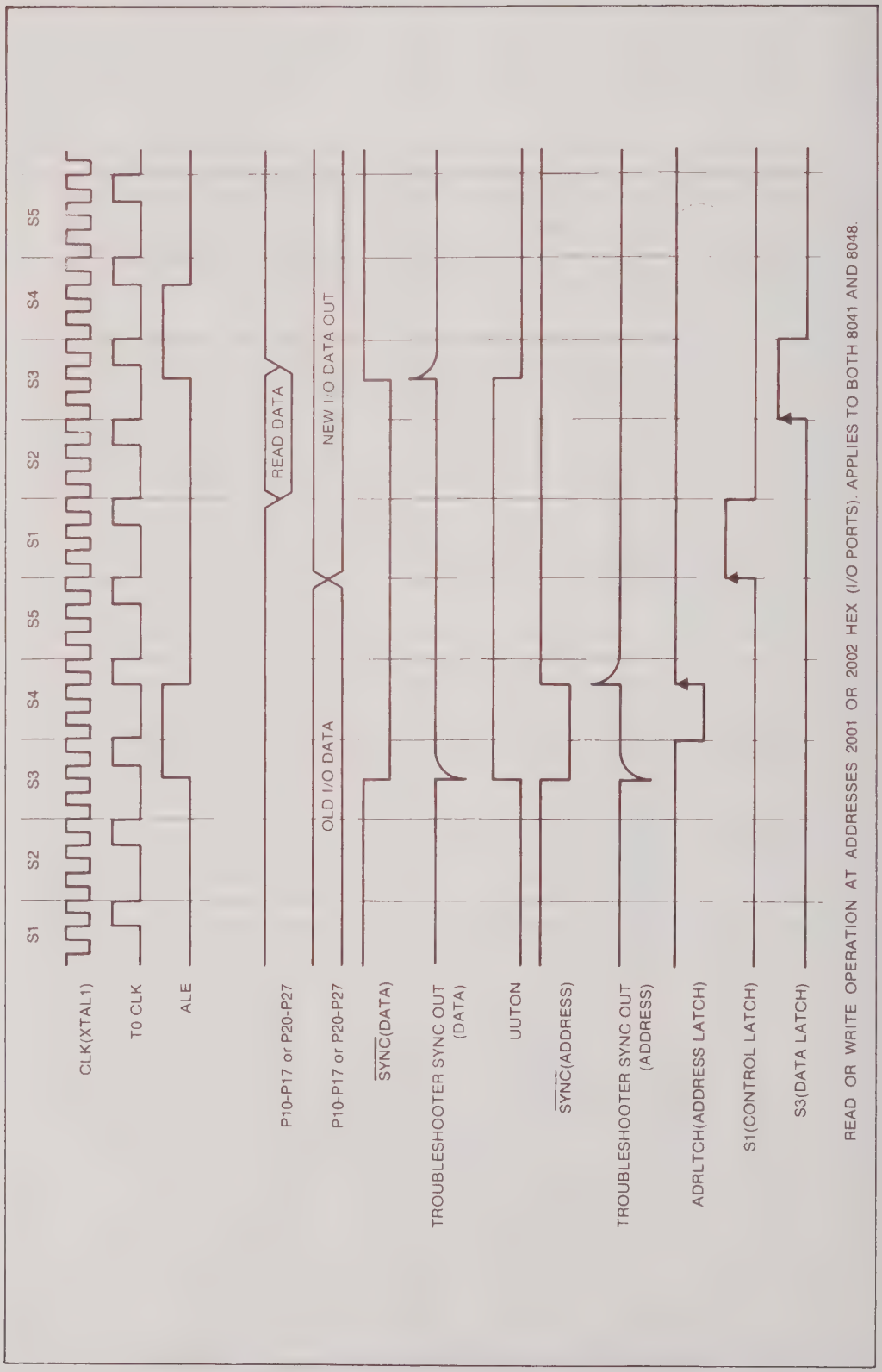


Figure 5-5. Examples of Signal Timing Relationships (cont)

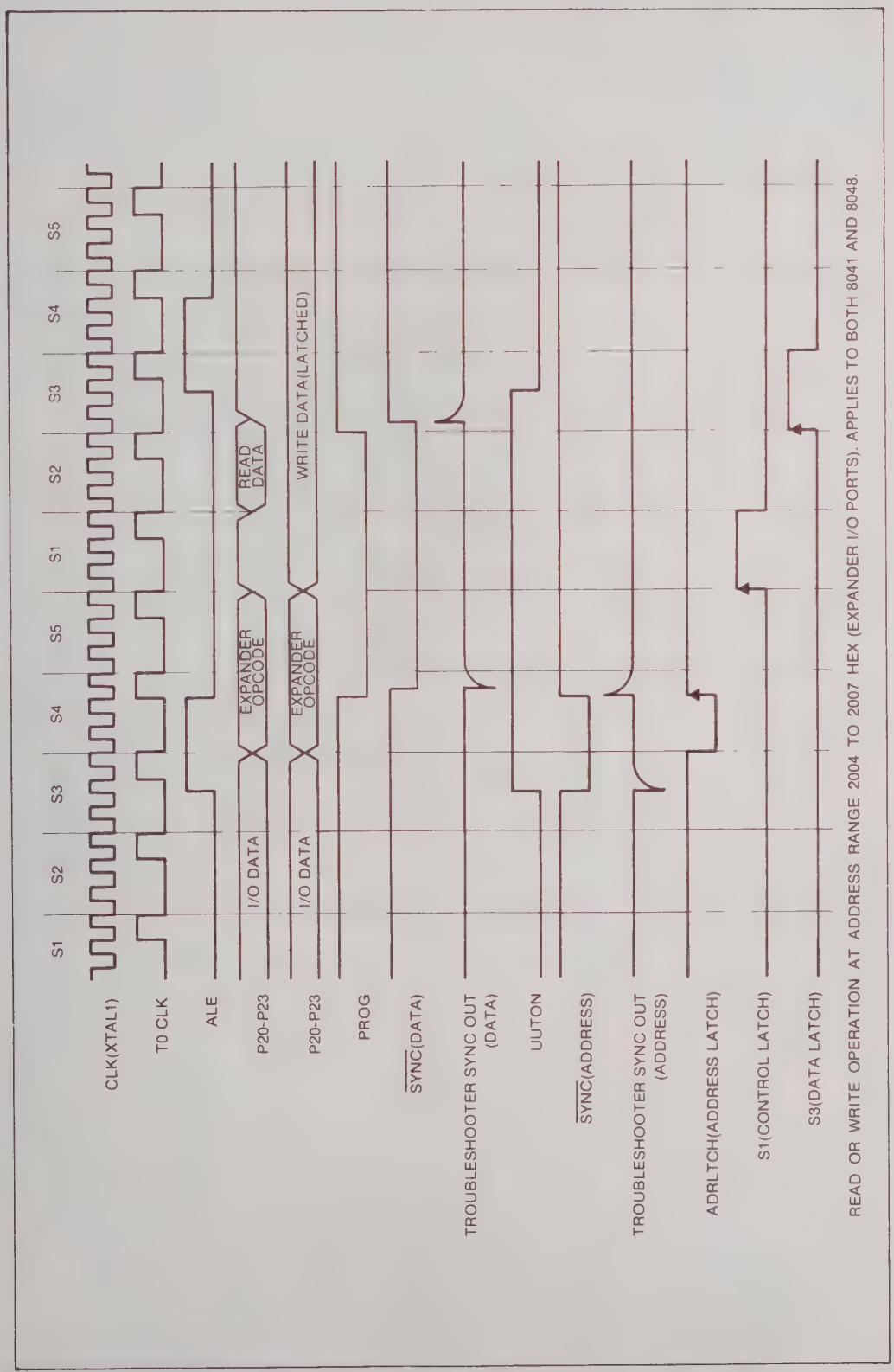


Figure 5-5. Examples of Signal Timing Relationships (cont)

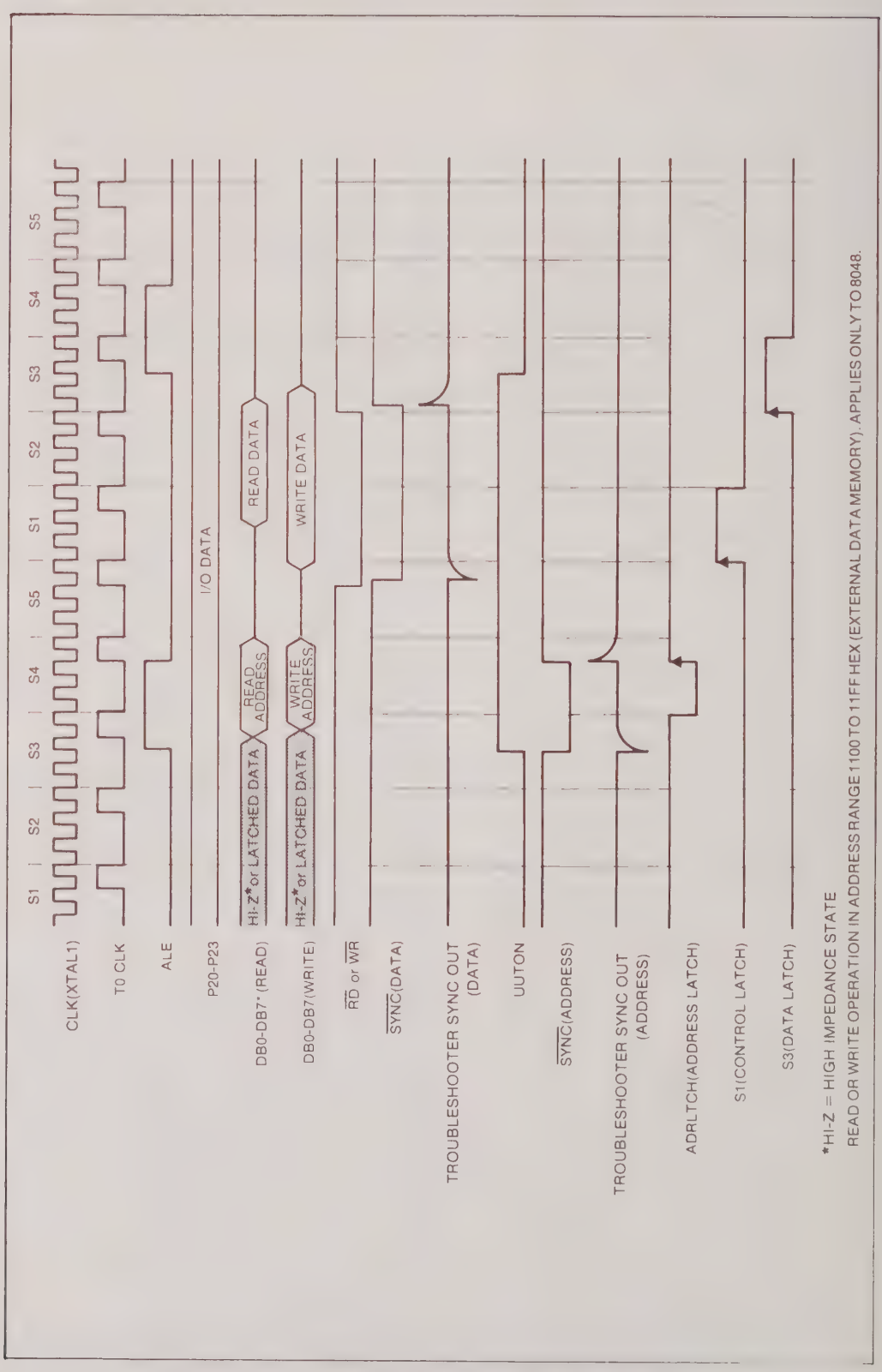
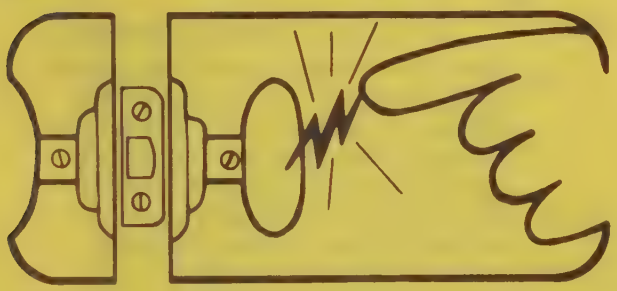


Figure 5-5. Examples of Signal Timing Relationships (cont)

static awareness

A Message From

John Fluke Mfg. Co., Inc.



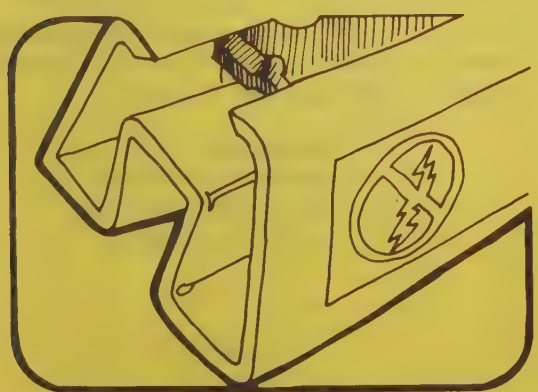
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

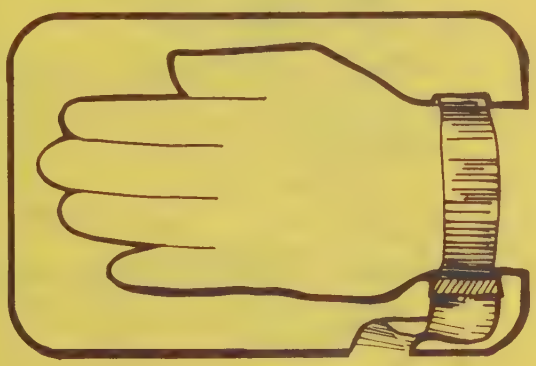
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗"

The following practices should be followed to minimize damage to S.S. devices.

1. MINIMIZE HANDLING

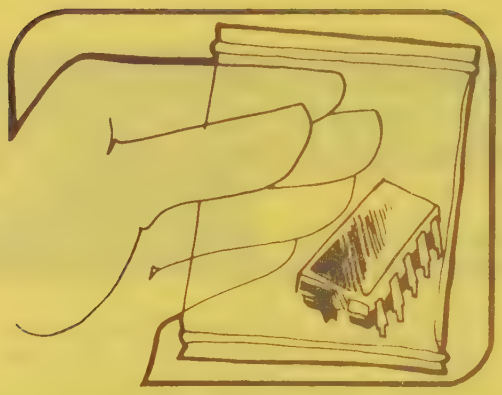


2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.

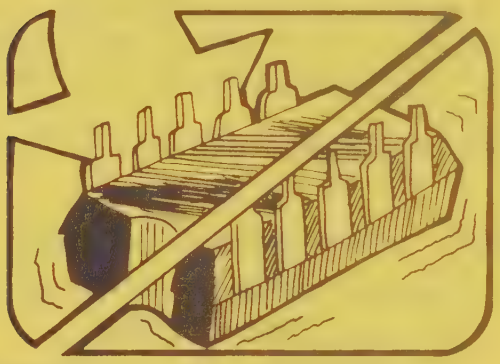


3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.

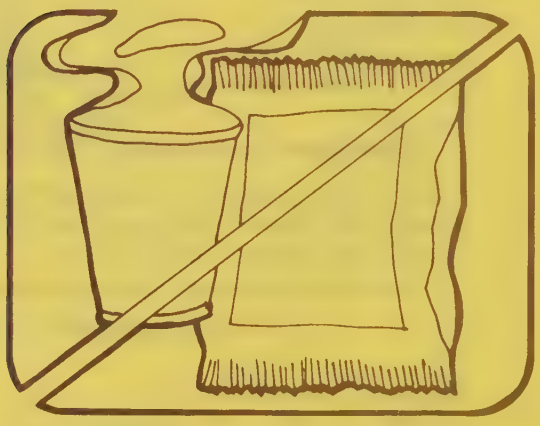
4. HANDLE S.S. DEVICES BY THE BODY



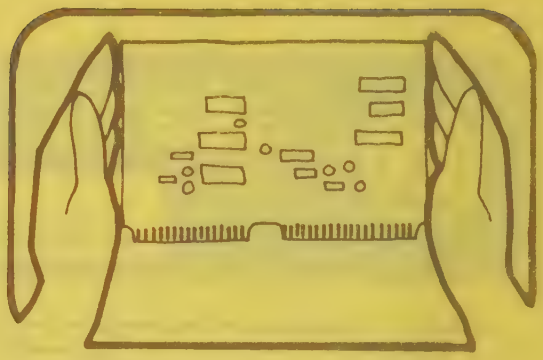
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



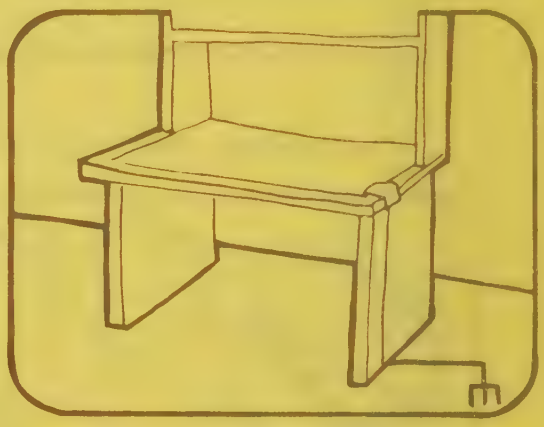
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

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Section 6
Troubleshooting

WARNING

THESE INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

6-1. INTRODUCTION

This section provides troubleshooting information for the pod. It includes repair precautions, disassembly procedures, and an adjustment procedure for the oscillator circuit.

The troubleshooting guidelines presented in this section are intended to assist in the isolation of faults within the pod. If you do not want to service the pod yourself, or if attempted troubleshooting fails to reveal the pod fault, you may ship the pod to the nearest Fluke Technical Service Center for repair. If requested, a free cost estimate will be provided before any repair work is performed. Refer to the troubleshooter operator or service manual for a list of Fluke Technical Service Centers.

If pod shipment is necessary, the pod should be shipped in its original shipping container if it is available. If the original shipping container is not available, you may order a new container from John Fluke Mfg. Co., Inc.; P.O. Box C9090, Everett, WA 98206; telephone (206) 342-6300.

Troubleshooting the pod is similar to troubleshooting any other microprocessor-based UUT, and requires the equipment listed in Table 6-1. The troubleshooting procedures provided in the following sections are supported by the theory of operation in Section 5 and the schematic diagrams in Section 8.

Table 6-1. Required Test Equipment for Pod Troubleshooting

EQUIPMENT TYPE	REQUIRED TYPE
Micro System Troubleshooter	Fluke 9000 Series
Interface Pod	Fluke 9000A-8048
Digital Multimeter	Fluke 8020
Oscilloscope	Tektronix 485 or equivalent
40 Pin IC Socket	

NOTE

All references to data and addresses in the following sections are in hexadecimal notation.

CAUTION

Static discharge can damage MOS components contained in the pod. To prevent this possibility, take the following precautions when troubleshooting and/or repairing the unit.

- Never remove, install, or otherwise connect or disconnect pcb (printed circuit board) assemblies without disconnecting the pod from the troubleshooter.
- Perform all repairs at a static-free work station.
- Do not handle ICs or pcb assemblies by their connectors.
- Wear a static ground strap when performing repair work.
- Use conductive foam to store replacement or removed ICs.
- Remove all plastic, vinyl, and styrofoam from the work area.
- Use a grounded soldering iron with a rating of 25 watts or less to prevent overheating the pcb assembly.
- When shipping the pod, always place the pod in a static-free plastic bag.

6-2. DETERMINING WHETHER THE POD IS DEFECTIVE OR INOPERATIVE

The first task of troubleshooting the pod is to determine whether the pod is defective or inoperative. This determination is based on the results of the pod self test described in Section 2. If you have not performed the self test, refer to Section 2 and perform the self test before proceeding with the troubleshooting.

Depending on the results of the pod self test and the pod behavior when connected to a known good UUT, the pod may be categorized in one of the three following groups:

- Defective Pod: The pod fails the pod self test and the troubleshooter displays a self test failure code. Refer to the section titled Troubleshooting a Defective Pod.
- Inoperative Pod: The pod is unable to complete the pod self test and the troubleshooter displays an *ATTEMPTING RESET* message. Refer to the section titled Troubleshooting an Inoperative Pod.
- Suspected Defective Pod: The pod passes the pod self test but exhibits abnormal behavior when connected to a known good UUT. Refer to the section titled Extended Troubleshooting Procedures.

6-3. WHAT HAPPENS DURING SELF TEST

Whenever pin 20 of the pod self test socket is connected to ground, the pod senses that it is in self test. Inserting the pod ribbon cable plug into the self test socket connects pin 20 to ground. The pod self test does not actually begin until the operator attempts an operation involving the pod and the pod informs the troubleshooter that it is in self test.

When the ribbon cable plug is inserted into the self test socket, the following electrical connections are made:

- The address/data bus lines DB0 through DB7 are connected to the I/O Ports, Port 1 (lines P10 through P17) and Port 2 (lines P20 through P27). This connection gives the pod a closed loop in which to read and write from each of the ports.
- The bus between the ports is also extended to include the status (input) lines. This allows each of the inputs to be exercised by a port line.
- A crystal is connected to the crystal inputs of the pod. This crystal replaces the clock source normally supplied by the UUT to operate the pod.
- All control lines are gated to an activity detector so that they may be individually tested for proper functioning.
- A +5V dc voltage is applied to pins 26 and 40 to simulate the UUT power supply and check the power fail sensing circuit.

6-4. TROUBLESHOOTING A DEFECTIVE POD

This section tells what to do if the troubleshooter displays the following message when the pod self test is performed: *POD SELF-TEST name FAIL xx (name = '35/48, '39/49, '40/50,* or *8041* depending on the microcomputer in the pod socket; *xx* represents the self test failure code). If instead the troubleshooter displays an *ATTEMPTING RESET* message, refer to the section titled Troubleshooting an Inoperative Pod.

The name that is reported by the troubleshooter during pod self test is a diagnostic message in itself. The Master Processor, Slave Processor, and Timing Section must be operating in order for the slave processor (installed by the operator in the external socket) to be properly identified. The microcomputer type is determined by the size of its internal RAM memory. The 8035 and 8048 microcomputers have 64 bytes of internal RAM, the 8039 and 8049 have 128 bytes, and the 8040 and 8050 have 256 bytes. In the case where the mode switch has been set to the 8041 mode, the name is reported as 8041 regardless of the type of microcomputer present in the socket.

Anytime the pod name reported by the troubleshooter during self test does not match the type of microcomputer installed in the socket, the microcomputer is probably defective. Obtain another 8048 family microcomputer, replace the suspected microcomputer in the socket, and perform the self test again. If the name is still incorrect, then the pod is probably defective.

6-5. Interpreting the Pod Self Test Failure Codes

The procedures for troubleshooting a defective pod are based on the information reported by the self test failure codes. In addition to the test routines that are performed on the pod by the troubleshooter in the standard pod self test routine, the pod has an internal enhanced self test which performs some more thorough test routines. The failure codes for the standard self test are listed in Table 6-2. The failure codes for the enhanced self test are listed in Table 6-3.

Whenever the pod self test is performed and the troubleshooter displays the message *POD SELF TEST* name *FAIL* xx where xx equals *01, 02,* or *03,* the pod failed the standard self test. Whenever the pod self test is performed and the troubleshooter displays the message *POD SELF TEST* name *FAIL 00,* the pod may have failed either the standard self test or the enhanced self test. In most cases the enhanced self test, which is more thorough, will detect the failure. (This enhanced self test is transparent to the

operator and to the troubleshooter; the troubleshooter does not know it is being performed.)

To find out if the pod failed the enhanced self test or the standard self test, perform a read operation at F0000. (F0000 is not an address within the normal address space of the pod microcomputer, but is a special address within the pod that contains information pertaining to the result of the enhanced self test). If the data returned is FF, then the pod passed the enhanced self test, which implies that any reported pod self test failures were caused by the failure of the standard self test. If the data returned is not FF, then the pod failed the enhanced self test.

For example, assume the pod self test is performed and the troubleshooter displays the message *POD SELF TEST* name *FAIL 02.* As shown in Table 6-2, the standard failure code 02 indicates that one or more control lines cannot be driven.

Table 6-2. Standard Pod Self Test Failure Codes

FAILURE CODE	DESCRIPTION
00*	UUT read access failed or the enhanced self test failed*
01	UUT write access failed
02	Control line(s) cannot be driven
03	Enableable status line(s) failed
*Code 00 may indicate the enhanced self test failed. To find out, perform a read at F0000 (while in self test). If the data returned is FF, the enhanced self test did not fail. If the data returned is anything other than FF, the enhanced self test failed; refer to Table 6-3 for the enhanced self test failure codes.	

Table 6-3. Enhanced Self Test Failure Codes

FAILURE CODE (DATA RETURNED BY READ @ F0000)	DESCRIPTION
00	The pod was able to initialize and communicate with the troubleshooter, but no tests were successfully performed.
01	Pod failed ROM test. The program ROM (U3) contents did not match the expected ROM signature when tested.
02	Pod failed internal RAM test. Not all bytes of the 8039 (U1) RAM memory were read/writeable.
03	Pod failed RAM test. Not all bytes of the 8155 (U13) RAM memory were read/writeable.
04	Pod failed UUT read/write test. One or more errors occurred during a series of diagnostic UUT reads and writes
FF	Pod passed all tests. No errors were detected.

For a second example, assume the pod self test is performed and the troubleshooter displays the message *POD SELF TEST* name *FAIL 00.* Notice in Table 6-2 that the standard failure code 00 may indicate that the enhanced self test failed. To check this possibility, perform a read operation at F0000 (while still in self test). Assume that the data returned by the read operation is 04. As shown in Table 6-3, the enhanced self test failure code 04 indicates that the pod failed a UUT read/write test.

For a third example, assume the pod self test is performed and the troubleshooter displays the message *POD SELF TEST* name *FAIL 00.* Perform a read operation at F0000 (while still in self test) to check whether the enhanced self test failed. Assume that the data returned by the read operation is FF. Data FF indicates that no errors were detected by the enhanced self test; as shown in Table 6-2, the only other possible cause for the original failure code 00 is that a UUT read access failed.

6-6. Preparing for Troubleshooting a Defective Pod

Prepare to troubleshoot your defective pod as follows:

1. If the pod is connected to a UUT, remove power from the UUT. Disconnect the pod from the UUT.

2. If the pod is connected to the troubleshooter, remove power from the troubleshooter. Disconnect the pod from the troubleshooter.

3. Refer to the later section titled Disassembly and disassemble the pod. It is not necessary to separate the two pcb assemblies at this time. The two pcb assemblies should remain securely fastened together with screws to avoid possible problems with electrical connections between the two pcb assemblies.

4. Look for any obvious problems such as burned components or ICs that are loose in their sockets. Replace components if necessary.

5. Obtain a 40-pin IC socket. Clip off or bend out of the way pin 20 of this socket. (You may use the socket saver that is supplied with the pod; the socket saver may be pried apart so you can remove pin 20). Insert the modified socket into the pod self test socket. Insert the pod ribbon cable plug into the modified socket as shown in Figure 6-1. Turn the adjacent thumbwheel to lock the self test socket.

6. Connect the pod to the troubleshooter.

7. Apply power to the troubleshooter.

8. Press the SETUP key on the troubleshooter and set the following conditions:

   SET-TRAP BAD POWER SUPPLY? YES

   SET-TRAP ILLEGAL ADDRESS? NO

   SET-TRAP ACTIVE INTERRUPT? NO

   SET-TRAP ACTIVE FORCE LINE? NO

   SET-TRAP CTL ERR? YES

   SET-TRAP ADDR ERR? YES

   SET-TRAP DATA ERR? YES

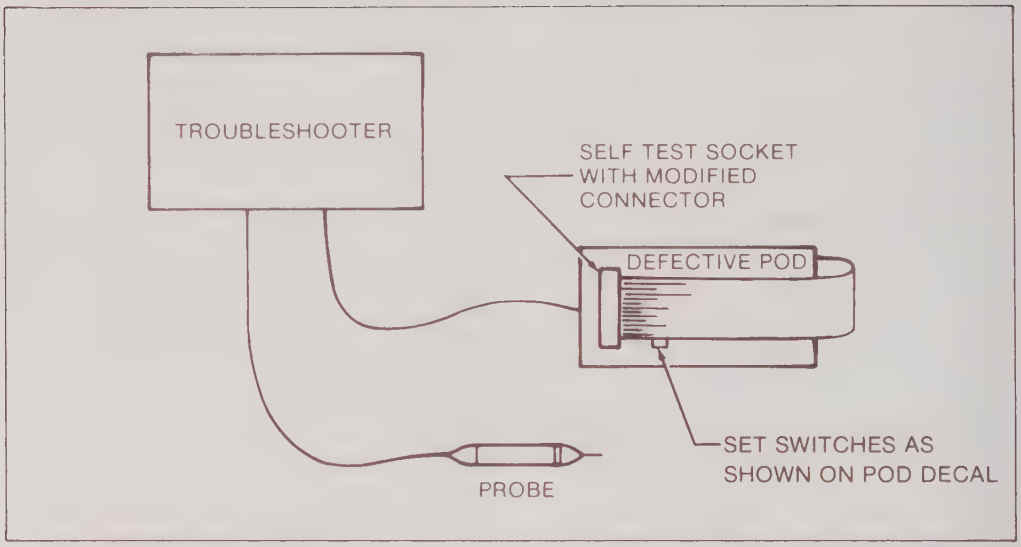


Figure 6-1. Troubleshooting a Defective Pod

When the pod and the troubleshooter are connected in this configuration, the tests and troubleshooting functions of the troubleshooter can be applied to the pod, much like any other UUT. (The troubleshooter does not know that the pod is plugged into itself.) Remember that in order to perform the pod self test, you must connect pin 20 of the self test socket to ground (or remove the modified socket) and then initiate a troubleshooter operation.

6-7. Procedure for Troubleshooting a Defective Pod

Now you are ready to proceed with troubleshooting. Note that the very fact that the self test was completed is a good indication that the problem is probably located in the UUT Interface Section of the pod. Since the self test was completed, the Master Processor, Slave Processor and the Timing Sections are probably functioning normally since they are essential for accepting the self test commands and communicating the results to the troubleshooter.

For most defective pods, the enhanced self test will detect the problem. The enhanced pod self test failure codes 00 through 03 indicate problems within the Master Processor section which are easily identified. Code 04, however, may be the result of any one of a multitude of different problems within the Slave Processor, the Timing and Control section, or the UUT Interface section. Further isolation of the problem may be possible by manually performing read and write operations to the various pod lines while the pod ribbon cable plug is installed in the self test socket.

While connected to the self test socket, Port 1, Port 2, the data bus and the status lines are all connected together (as shown in the schematic in Section 8). This configuration allows data to be written back and forth from one port to another. Data presented on the common bus may be read on the status inputs to verify their proper functioning. Using this method, open and shorted lines and/or buffers may be readily isolated.

The following sequence of instructions may be used to troubleshoot a defective pod. The steps should be performed in sequence since subsequent steps require the data supplied by preceeding steps. When a step is performed which does not produce the expected results, loop on that test and locate the source of the error.

1. Make sure the pod and troubleshooter are prepared for troubleshooting as described in the previous section.

2. Set the mode switch to the 8048 mode. All of the lines of the pod may be tested when set up in this configuration. Port 1 and Port 2 are in the input mode. The data bus (DB0 through DB7) is in the high impedence state. ALE should be the only active control line.

3. Perform a *READ @ 2001;* data returned should be FF. (Port 1 and Port 2 are pulled to logic high values in the input mode.) This test should help locate lines which are shorted to ground.

4. Perform a *READ @ STATUS;* data returned should be 3F. The data present on the bus (all lines are still pulled high by Port 1 and Port 2) is read on the status inputs. This test verifies that the status lines properly input a high value.

5. Perform a *WRITE @ 2000 = 00.* This operation latches a low value output on each of the data lines. This tests the data bus output buffers (U2) and checks for stuck high lines.

6. Perform a *READ @ STATUS;* data returned should be 00. With all of the data lines driven low, the status inputs should also indicate low values. This test will help locate open status lines.

7. Perform a *READ @ 2000;* data returned should be 00. This verifies that the input buffers of the data bus (U1) are functioning properly.

8. Perform a *READ @ 2001;* data returned should be 00. Lines with a high value indicated are likely to be open.

9. Perform a *READ @ 2002;* data returned should be 00. This operation tests for open lines and for proper functioning of the Port 2 input buffers.

10. Perform a *WRITE @ 2001 = FF.* Verify that this results in a data error at 2001 with bits FF. This tests the drivability sampling circuits of Port 1 (P10 through P17). Port 1 only outputs the high value momentarily and then returns to the input mode.

11. Perform a *WRITE @ 2002 = FF.* Verify that this results in data error at 2002 with bits FF. This tests the drivability sampling circuits of Port 2 (P20 through P27). Port 2, like Port 1, only outputs the high value momentarily and then returns to the input mode.

12. Perform a *WRITE @ 2000 = 55.* A data error here indicates that adjacent lines are shorted.

13. Perform a *WRITE @ 2000 = AA.* A data error here indicates that adjacent lines are shorted.

14. Perform a *READ @ 00F.* Verify that this results in an address error at 00F with bits F00, and that the data returned is 00. This tests the address drivability sampling circuits.

15. Perform a Bus Test. Verify that address lines A0 through A3 are tied to address lines A8 through A11 respectively. This also tests the address drivability sampling circuits.

16. Perform a *READ@2004;* data returned should be 0F. This test verifies proper functioning of the Port 2 buffers when performing an expander I/O operation.

One other thing to check is the oscillator circuit. The oscillator circuit has a potentiometer (R24 on the interface board) which can be used to adjust the clock signal that is sent to the slave processor (U30 on the processor board). To check the clock signal, place the oscilloscope probe at pin 2 of U30. If the signal is not +5.0V p-p, refer to the later section titled Oscillator Circuit Adjustment Procedure and adjust the oscillator circuit.

6-8. TROUBLESHOOTING AN INOPERATIVE POD

6-9. Introduction

This section describes what to do if the troubleshooter displays any of the three *ATTEMPTING RESET* messages when the pod self test is performed. The *ATTEMPTING RESET* messages indicate that the pod is not operating and is not responding to the troubleshooter.

NOTE

When performing the pod self test, make sure that the troubleshooter power is on, the pod is connected to the troubleshooter, a properly functioning 8048 family microcomputer is installed in the pod (with the socket locked), and the pod ribbon cable plug is installed in the self test socket (with the socket locked).

If you correct a problem while using the procedures provided in this section, try the pod self test again. If the troubleshooter again displays an *ATTEMPTING RESET* message, continue with the procedures in this section. However, if the troubleshooter displays the message *POD SELF-TEST* name *FAIL* xx, refer to the previous section titled Troubleshooting a Defective Pod. The reason for referring to the other section is that when the pod is again communicating with the troubleshooter, you may use the pod to help troubleshoot itself.

The procedures in this section apply primarily to the Processor and Timing Sections. (The Processor and Timing Sections are described in the theory of operation in Section 5.)

6-10. Preparation for Troubleshooting an Inoperative Pod

An inoperative pod is like any other microcomputer-based UUT that is not operating properly; the easiest way to fix an inoperative pod is by using a troubleshooter and a good pod. Prepare to troubleshoot the pod by performing the following steps:

1. If the pod is connected to a UUT, remove power from the UUT. Disconnect the pod from the UUT.

2. If the pod is connected to the troubleshooter, remove power from the troubleshooter. Disconnect the pod from the troubleshooter.

3. Refer to the later section titled Disassembly, and disassemble the pod.

4. Look for any obvious problems such as burned components or ICs that are loose in their sockets. Replace components if necessary.

5. Remove the pod microcomputer (U1) from its socket.

6. To provide a clock signal for the inoperative pod, insert the inoperative pod ribbon cable into the inoperative pod self test socket. (Make sure the clock is working properly; an alternative source for a clock signal is a known good UUT.)

7. If a second troubleshooter is available, connect the pod cable plug from the inoperative pod to the second troubleshooter to supply the inoperative pod with power. If a second troubleshooter is not available, connect a +5V dc (2A) power supply and a –5V dc (200 mA) power supply to the inoperative pod as shown in Figure 6-2. An easy place to make the power connections is at the connector that usually connects the cable to the troubleshooter. Connect pins 2 and 15 to +5V, pin 21 to –5V, and pin 25 to ground.

8. Connect the troubleshooter to the good pod as shown in Figure 6-2. Apply power to the troubleshooter, then install the ribbon cable plug of the good pod in the microcomputer socket of the inoperative pod.

CAUTION

Do not apply or remove power with the ribbon cable connected between the good pod and the inoperative pod.

CAUTION

Do not separate the pcb assemblies of the inoperative pod with power applied to the inoperative pod. Failure to comply with this can damage CMOS components in the pod. The pcb assemblies should be securely fastened together with the proper screws before applying power.

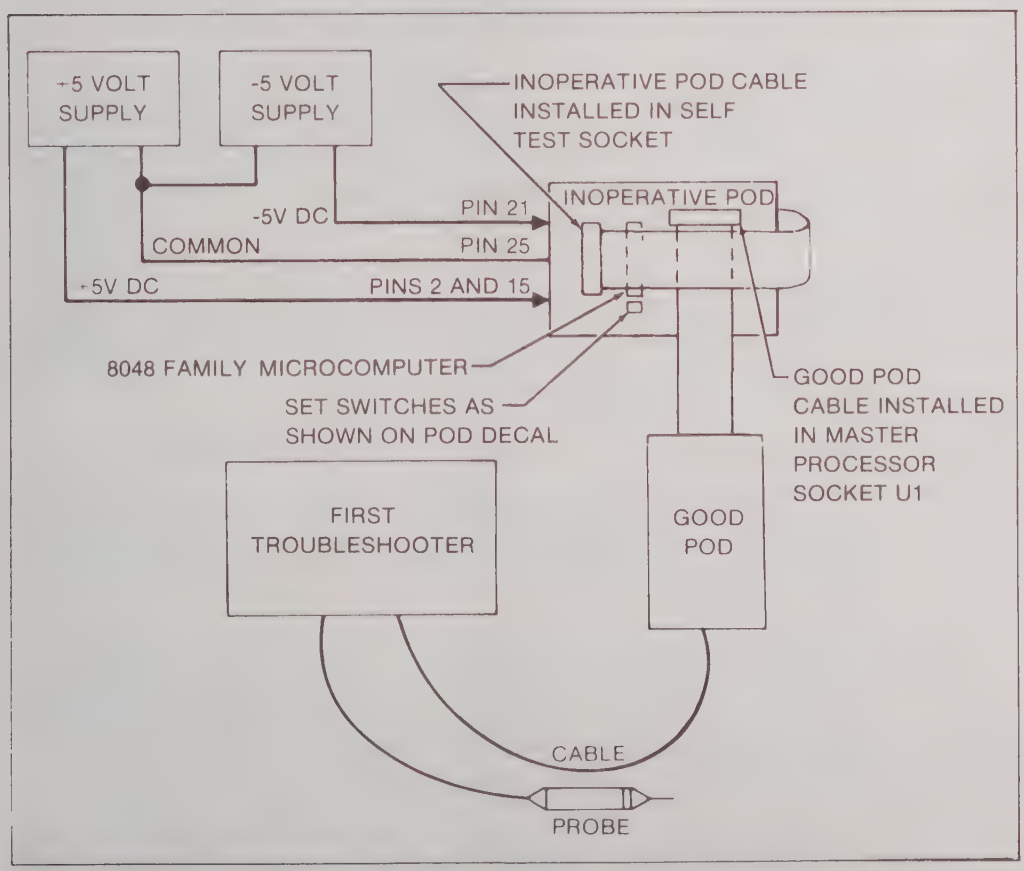


Figure 6-2. Troubleshooting an Inoperative Pod

6-11. Procedure for Troubleshooting an Inoperative Pod

Use the following steps as a guide for troubleshooting an inoperative pod. The circuits and components mentioned in these steps appear in the schematic diagrams in Section 8, and the circuits are described in the theory of operation in Section 5.

The procedures in the following steps are designed to check the operation of all the circuits that enable the pod to communicate with the troubleshooter. When you are able to successfully complete all of the steps, the troubleshooter should no longer display a *POD TIMEOUT* message but should be able to communicate with the pod.

When the pod begins to respond to the troubleshooter, perform the pod self test to see if the pod is operating properly. If the pod is able to complete the self test but does not pass, continue troubleshooting using the procedures listed in the previous section titled Troubleshooting a Defective Pod.

1. Press the SETUP key on the troubleshooter and select the Setup message *SET-TRAP ACTIVE FORCE LINE? NO.*

NOTE

The following steps test all the lines directly connected to the master processor (U1).

2. Perform either Step a or Step b as follows:

   a. If a second troubleshooter is being used, do the following:

      1. Press the SETUP key on the second troubleshooter, select the Setup message *SET-TIMEOUT* xxx-*CHANGE?,* and set the timeout delay value to 100. Press the BUS TEST key on the second troubleshooter, which should display a *POD TIMEOUT* message. On the first troubleshooter, perform a read at 2001 and verify that the data value AB is received. This checks the operation of the lines POD0 through POD7.

      2. On the first troubleshooter, perform a Read Status operation and press LOOP. Bits 1 and 4 (corresponding to lines $\overline{\text{Reset}}$ and T0) should be 1 most of the time, with an occasional display of 0. Bits 0 and 5 (corresponding to lines EA and $\overline{\text{SS}}$) should display a constant value of 1. This verifies that the lines $\overline{\text{Reset}}$, T0, EA, and $\overline{\text{SS}}$ are functioning properly.

   b. If a second troubleshooter is not being used, do the following:

      1. Select the data sync mode. Use the stimulus capability of the probe to apply pulses to each of the data lines POD0 through POD7 at the connector J1 while performing the operation *READ @ 2001 LOOP.* Verify that each of the data lines is working.

      2. Perform a Read Status operation and press LOOP. Use the stimulus capability of the probe to pulse the $\overline{\text{Reset}}$ and $\overline{\text{MAINSTAT}}$ lines at J1. Verify that the $\overline{\text{Reset}}$ and T0 bits receive the intended data. Verify that the EA and $\overline{\text{SS}}$ lines display a constant value of 1. This verifies that the $\overline{\text{Reset}}$, T0, EA and $\overline{\text{SS}}$ lines are functioning properly.

3. If it is not yet selected, select the data sync mode. Place the probe on U13-7 and perform the operation *DTOG @ 2002 = FE BIT 0.* Verify that the node goes high, then low and remains low. This checks the path of P20 through U10.

4. Place the probe on U13-4. Perform the operation *DTOG @ 2002 = FF BIT 4.* Verify that the node goes low, then high and stays high. Place the probe on U30-4 and perform the operation *READ @ 2002.* Verify that the node is low. This test assures that the 8155 PIA and the slave processor are reset properly.

5. Setup the 8155 PIA by performing the operations *WRITE@2002=F3, WRITE @1100 = 4F, WRITE @ 1101 = 02.* Then probe the node at U30-5. Perform the operation *DTOG@2002=FF BIT 5.* Verify that this node goes low, then high and stays high. Keep the probe at the same point and perform the operation *DTOG@ 2002=FF BIT 6.* The probe should indicate a low followed by high. Repeat this test (toggle both bits) while probing U9-19 and U16-19. The signal at U9-19 should go low, then high and stay high. The signal at U16-19 should go high, then low and stay low. This step tests the enable control lines of the buffers on the shared bus and the single step control to the slave processor.

6. Perform the operation *DTOG @ 2002 = FF BIT 7 LOOP.* If a second troubleshooter is connected to the inoperative pod, it should display the message *POD RESET ERR - ATTEMPTING RESET.* If a second troubleshooter is not being used, probe pin 24 of J1 and verify that the signal is toggling. This test verifies that the $\overline{\text{PODSTAT}}$ signal is working.

7. While performing a Read Status operation, open the self test socket of the inoperative pod and remove the pod cable. Verify that the $\overline{\text{INT}}$ line is low while the socket is open. This checks that the power fail sensing circuit and $\overline{\text{INT}}$ line are working properly. Reinstall the pod cable in the self test socket.

8. Place the probe at U28-1. Perform the operation Read @ 2004 and verify that the signal is low. Perform the operation Read @ 2001 and verify that the signal is high. This tests that the MPROG line is continuous to U28.

9. Place the probe at U13-9. Perform the operation Read @ 1100. Repeat with the probe at U9-1. Verify that in both cases the signal is low. This assures that the $\overline{\text{MRD}}$ line is functioning properly.

10. While probing U13-10, perform the operation Write @ 1100 = 00. Verify that the signal is low. This test verifies that the $\overline{\text{MWR}}$ signal is continuous to the 8155 PIA.

11. Place the probe at U3-20 and perform the operation Read @ 0000. Verify that the signal is low. The $\overline{\text{MPSEN}}$ line is checked in this test.

12. Using the stimulus mode of the probe to generate toggling pulses, pulse U14-13 and perform a Read Status operation. Verify that line T1 toggles. This test checks the single step and step completion feedback circuits. Turn off the probe stimulus mode before continuing.

NOTE

The following test verifies that the program memory is accessible and is functioning properly.

13. Perform the operation *ROM TEST @ 300-383 SIG A040.* This test checks the address latch (U2), the ROM (U3), and the interconnecting address and data lines.

NOTE

The next test determines whether the RAM memory is working properly.

14. Perform the operation *WRITE @ 2002 = F2.* This operation selects the RAM memory of the 8155 PIA. Perform the operation *RAM SHORT (or RAM LONG) @ 1100-11FF.* This verifies the RAM of the 8155 PIA.

NOTE

The following tests verify several essential I/O lines.

15. Set up the 8155 PIA for the I/O tests as follows: perform a *WRITE @ 2002 = F3;* this selects the 8155 I/O. Then perform a *WRITE @ 1100 = 4F;* this writes to the 8155 control register and configures Ports A, B and C as outputs.

16. Perform the operation *I/O TEST @ 1101-1102 BTS FF.* Then perform the operation *I/O TEST @ 1103 BTS 3F.* This test verifies that the 8155 I/O ports are read/writable.

17. Place the probe at U19-1. Perform the operation *DTOG @ 1101 = 02 BIT 0.* Verify that the node goes high, then goes low and stays low. This verifies that the ENUUT line functions properly.

18. With the probe placed at U30-4, perform the operation *DTOG @ 1102 = 08 BIT 3.* The signal should go high, then go low and stay low. This operation verifies that the slave processor can be reset.

NOTE

The next test allows the slave processor to execute a very simple program in free-run. By checking the signal at each of the slave processor pins and comparing the signal to expected results, the slave processor section may be verified.

19. Perform the operation Write @ 2002 = F2. This selects the 8155 RAM which will contain the program for the simple test. Perform the operations Write @ 1100 = 75, Write @ 1101 = 04, Write @ 1102 = 00. This is a short program which enables the T0 clock output then jumps back to the beginning and enables it again. Perform the operation Write @ 2002 = B2; this operation releases the slave processor from the single step mode and allows it to perform the program in free-run. Select the free-run sync mode and use the probe to verify that each of the signals on the slave processor (U30 on the processor pcb assembly) have the logic levels listed in Table 6-4.

NOTE

The next step checks the clock signal from the oscillator circuit.

20. Place the oscilloscope probe at pin 2 of the slave processor (U30 on the processor pcb assembly). If the signal is not +5.0V p-p, refer to the later section titled Oscillator Circuit Adjustment Procedure and adjust the oscillator circuit.

NOTE

If any repairs are made to the oscillator circuit, the circuit will need to be adjusted. Refer to the section titled Oscillator Circuit Adjustment Procedure.

Table 6-4. Signal Levels at Slave Processor (U30) Pins

PIN NUMBER	LOGIC LEVEL OF SIGNAL	PIN NUMBER	LOGIC LEVEL OF SIGNAL
1	High and Low	21	High and Low
2	High and Low	22	High and Low
3	High and Low	23	High and Low
4	High	24	High and Low
5	High	25	High
6	X	26	High
7	High	27	X
8	High	28	X
9	High and Low	29	X
10	High	30	X
11	High and Low	31	X
12	High and Low	32	X
13	High and Low	33	X
14	High and Low	34	X
15	High and Low	35	X
16	High and Low	36	X
17	High and Low	37	X
18	High and Low	38	X
19	X	39	X
20	Low	40	High

X = don't care

If any repairs have been made to the inoperative pod as a result of the preceeding steps, try the pod self test again. If the pod passes the self test, the problems are probably corrected. If the pod fails the self test but is operating well enough to complete the test, refer to the previous section titled Troubleshooting a Defective Pod.

6-12. EXTENDED TROUBLESHOOTING PROCEDURES

The troubleshooting procedures provided in this section supplement the circuit checks performed on the pod during the pod self test; these procedures are appropriate for use with a pod that passes the pod self test but does not appear to function normally when used with a troubleshooter and a good UUT. If a pod fails the self test, it would be better to begin troubleshooting with the procedure provided in the previous section titled Troubleshooting a Defective Pod.

6-13. Erroneous Reporting or Non-Reporting of Drivability Errors

Drivability errors are detected by signals that are taken from the hybrid protection circuits A1 through A5. To troubleshoot this kind of problem, begin by performing the troubleshooter operation which does not work correctly. Use the LOOP key to repeat the error. With the probe set to the proper synchronization mode, check the logic levels present on the sampling latch side of the hybrids. This test should detect whether any hybrids are open or short-circuited. If the proper data is present at this point then it is likely that the associated sampling latch (U3 through U9) is defective.

6-14. Timing Problems

These problems are usually caused by components that are still functioning, but are not functioning within the allowable specifications. The best way to check this problem is to look at suspected signals using an oscilloscope synchronized to valid addresses. Look for

slow rise or fall times or signals driven to marginal logic levels. If the component is responding too slowly, it might fail with the UUT but pass the pod self test because the pod clock rate is slightly slower.

6-15. Run UUT Timing Problems

Occasionally a problem occurs when a pod seems to test a UUT properly but fails to perform successfully in the Run UUT mode. This type of problem may be related to the timing problems mentioned in the previous section. A UUT which operates marginally with respect to capacitive loading, DC loading, or timing may pass the troubleshooting tests, but fail in the Run UUT mode. Failure in the Run UUT mode may be due in part to the fact that the lines T0 and P20 through P23 are switched through buffers during normal testing, and switched through analog switches during the Run UUT mode. These lines have a total series resistance of approximately 200 ohms due to the protection networks and the analog switches. With a resistive load and an oscilloscope, the resistance of these lines may be checked to verify that they are not excessive. If the lines do not have excessive resistance, then the design margins of the UUT are probably not sufficient to allow the pod to perform in the Run UUT mode.

6-16. Noise Problems

If a part has marginal drive capabilities, the added noise of a UUT environment might cause it to fail. Note that inputs can malfunction (they may exhibit excessive leakage) and put too much load on an output causing either low signal levels, slow transition times, or both.

6-17. OSCILLATOR CIRCUIT ADJUSTMENT PROCEDURE

The oscillator circuit has a potentiometer (R24 on the interface pcb assembly) which controls the adjustment of the clock signal to the slave processor (U30 on the processor board). The following steps describe the procedure for performing the adjustment. This adjustment should be performed whenever the oscillator circuit has been repaired.

1. Remove power from the troubleshooter. Refer to the section titled Disassembly and disassemble the pod (the two pcb assemblies do not need to be separated).

2. Locate potentiometer R24 on the interface pcb assembly (as shown in Figure 6-3) and turn R24 fully counter-clockwise.

3. Insert the pod ribbon cable plug into the self test socket and lock the socket. The self test socket will provide the crystal source for the oscillator circuit.

4. Turn on the troubleshooter power.

5. Place an oscilloscope probe as indicated in Figure 6-3 (either U30-2 on the processor pcb assembly, or at TP3 on the interface pcb assembly).

6. Slowly turn R24 clockwise until the signal as shown on the oscilloscope is +5.0V p-p. This completes the adjustment procedure.

6-18. DISASSEMBLY

To gain access to the two pcb assemblies in the pod, perform the following steps:

1. Remove the pod ribbon cable plug from the self test socket.

2. Turn the pod over on its top (with the large pod decal facing up). Remove the four phillips screws that hold the case halves together and remove the top and bottom case halves. Place the pcb assemblies so that the self test socket (on the processor pcb assembly) is facing up.

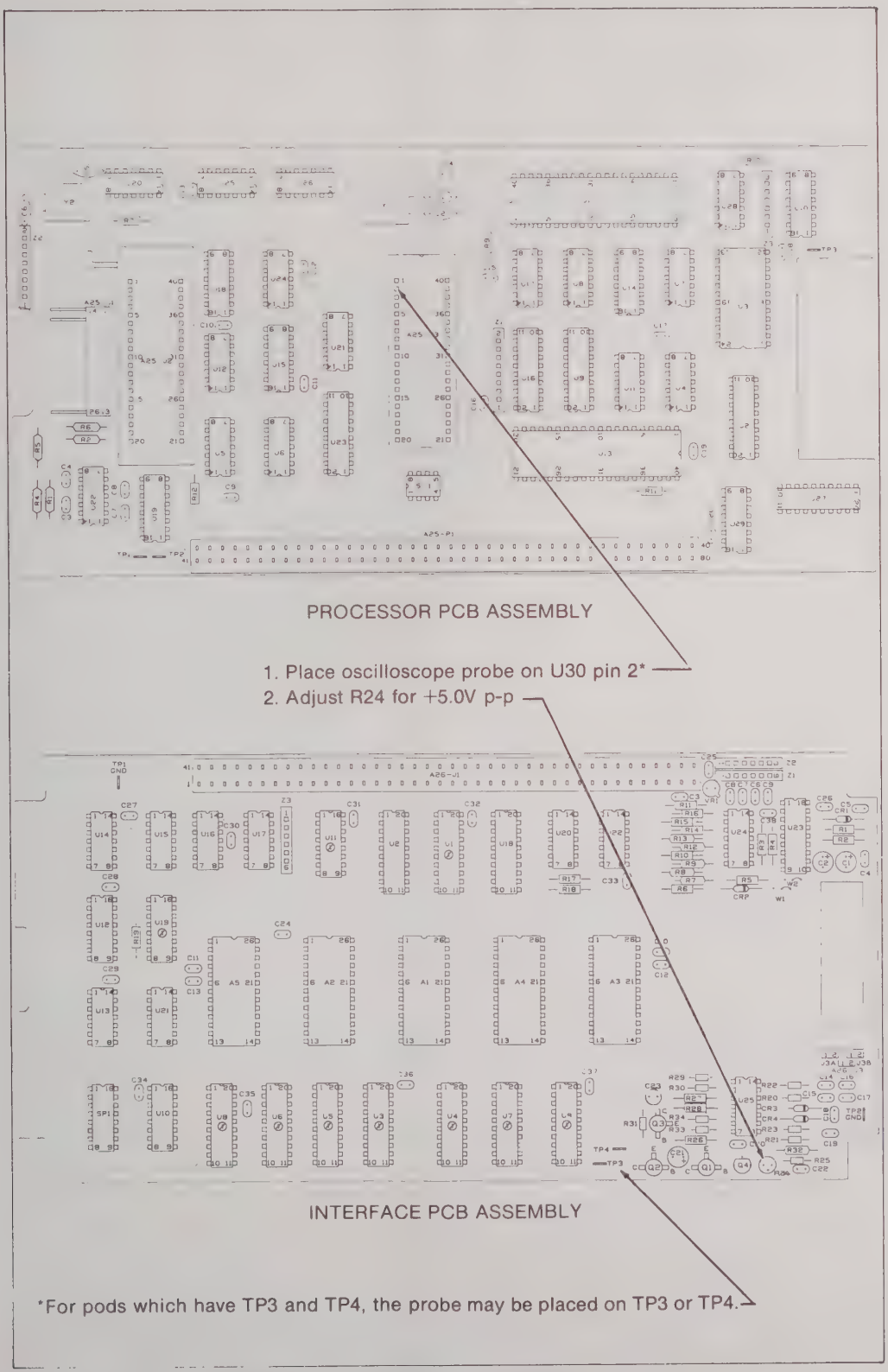

PROCESSOR PCB ASSEMBLY
1. Place oscilloscope probe on U30 pin 2*
2. Adjust R24 for +5.0V p-p
INTERFACE PCB ASSEMBLY
*For pods which have TP3 and TP4, the probe may be placed on TP3 or TP4.

Figure 6-3. Oscillator Circuit Adjustment Location

3. On the corner opposite the self test socket thumbwheel, remove the single phillips screw that retains the shield surrounding the pcb assemblies. (A standoff and washer will come off with the screw.) Remove the shield.

NOTE

When the shield is removed, all the components are exposed. It may not be necessary to separate the two pcb assemblies while troubleshooting except to replace components. If the two pcb assemblies are not separated, be sure that they are securely screwed together to ensure proper electrical connection.

4. To separate the two pcb assemblies, turn the pcb assemblies over so that the self test socket is facing down. Remove the four phillips screws at the corners of the pcb assemblies and carefully pull the boards apart at the two connectors along the sides.

Section 7
List of Replaceable Parts

7-1. INTRODUCTION

This section contains an illustrated parts list for the instrument. Components are listed alphanumerically by assembly.

Parts lists include the following information:

1. Reference Designation.

2. Description of Each Part.

3. Fluke Stock Number.

4. Federal Supply Code for Manufacturers (see the 9000 Series Troubleshooter Service Manual for Code-to-Name list).

5. Manufacturer's Part Number.

6. Total Quantity of Components Per Assembly.

7. Recommended quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of 2 years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for 1 year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked.

7-2. HOW TO OBTAIN PARTS

Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. or an authorized representative by using the Fluke Stock Number.

In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Quantity.

2. Fluke Stock Number.

3. Description.

4. Reference Designation.

5. Printed Circuit Board Part Number and Revision Letter.

6. Instrument Model and Serial Number.

A Recommended Spare Parts Kit for your basic instrument is available from the factory. This kit contains those items listed in the REC QTY column for the parts lists in the quantities recommended.

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representative. Prices are also available in a Fluke Replacement Parts Catalog, which is available upon request.

CAUTION

Indicated devices are subject to damage by static discharge.

7-3. MANUAL CHANGE AND BACKDATING INFORMATION

Table 7-4 contains information necessary to backdate the manual to conform with earlier pcb configurations. To identify the configuration of the pcbs used in your instrument, refer to the revision letter on the component side of each pcb assembly.

As changes and improvements are made to the instrument, they are identified by incrementing the revision letter marked on the affected pcb assembly. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

To backdate this manual to conform with an earlier assembly revision level, perform the changes indicated in Table 7-4. There are no backdating changes at this printing. All pcb assemblies are documented at their original revision level.

Table 7-1. 9000A-8048 Final Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
	⊘FINAL ASSEMBLY, 9000A-8048 POD FIGURE 7-1 (9000A-8048-5001)						
A25⊘	PROCESSOR PCB ASSEMBLY	647941	89536	647941	1		
A26⊘	INTERFACE PCB ASSEMBLY	647958	89536	647958	1		
H1	SCREW, PHP, 4-40 X 1/4	185918	89536	185918	4		
H2	SCREW, PHP, 4-40 X 5/8	145813	89536	145813	1		
H3	SCREW, RHP, 4-40 X 3/4	115063	89536	115063	4		
H4	WASHER, #4 LOCK	110403	89536	110403	1		
MP1	ACTUATOR	582916	89536	582916	1		
MP2	COVER, SLIDE	653139	89536	653139	1		
MP3	DECAL, POD	659177	89536	659177	1		
MP4	DECAL, SPECIFICATION	659169	89536	659169	1		
MP5	DECAL, SWITCHING	680421	89536	680421	1		
MP6	DECAL, WARNING	659813	89536	659813	1		
MP7	LABEL, STATIC CAUTION	605808	89536	605808	1		
MP8	LABEL, UUT CAUTION	634030	89536	634030	1		
MP9	SHELL, BOTTOM	648881	89536	648881	1		
MP10	SHELL, TOP	653113	89536	653113	1		
MP11	SHIELD	659771	89536	659771	1		
MP12	SPACER, HEX	187575	89536	187575	1		
MP13	9000A POD ASSCESSORIES (NOT SHOWN)	607176	89536	607176	1		
	FOAM CUSHION				1		
	LABEL, UUT CAUTION				1		
	PLASTIC BAG, ASSCESSORY				1		
	SOCKET, DIP 40-PIN (SOCKET SAVER)	614297	89536	614297	2		
TM1	INSTRUCTION, MANUAL (9000A-8048)	649418	89536	649418			
U3	IC, EPROM	582213	89536	582213	1	1	
U23	IC, PAL	609255	89536	609255	1	1	
U27	IC, PAL	611806	89536	611806	1	1	
U30	IC, 8-BIT MICROCOMPUTER	504563	34649	8039	1	1	
W1	CABLE, POD (TO J1)	581819	89536	581819	1		
W2	CABLE, UUT (TO J2)	680595	89536	680595	1		
	RECOMMENDED SPARE PARTS KIT	653501	89536	653501			

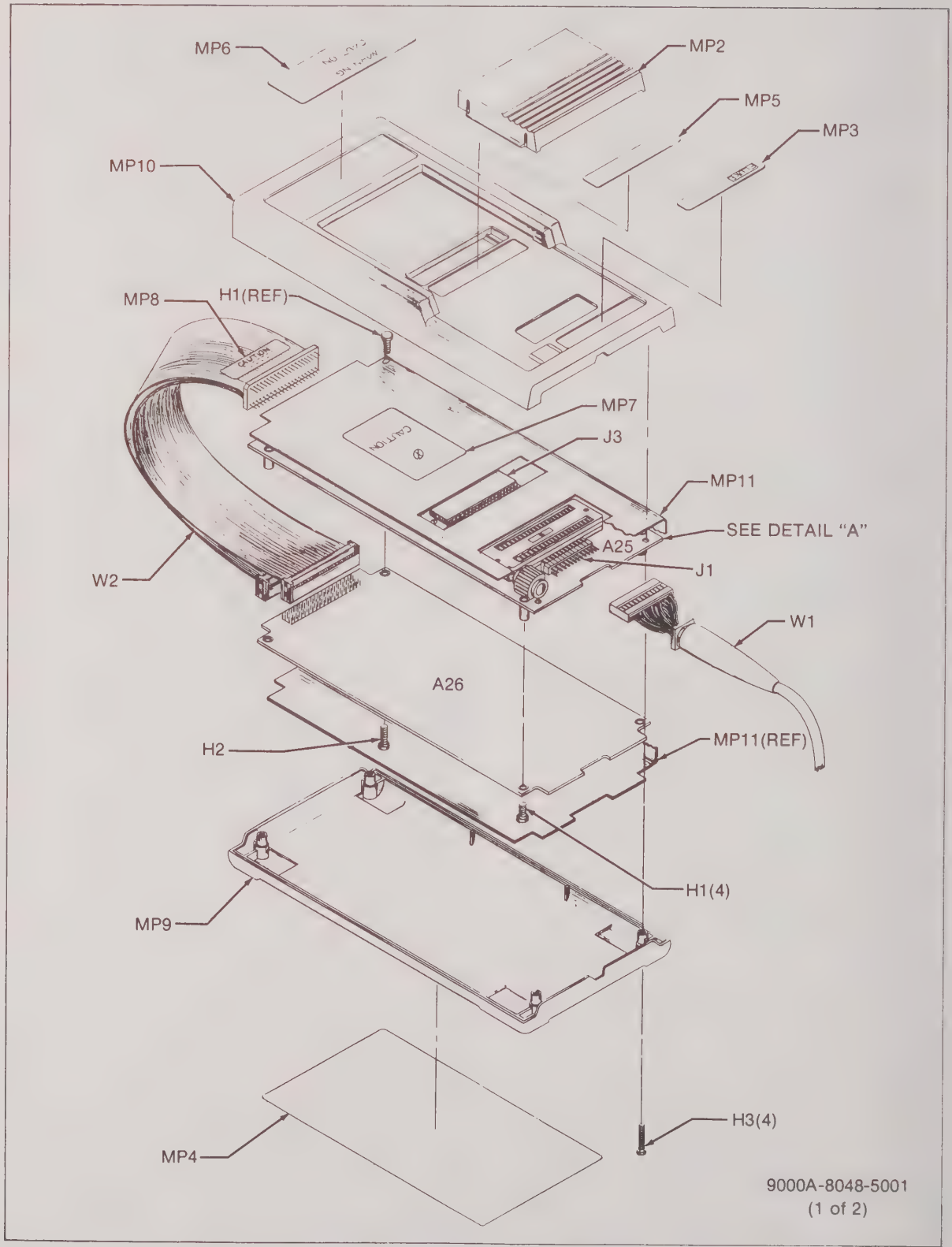
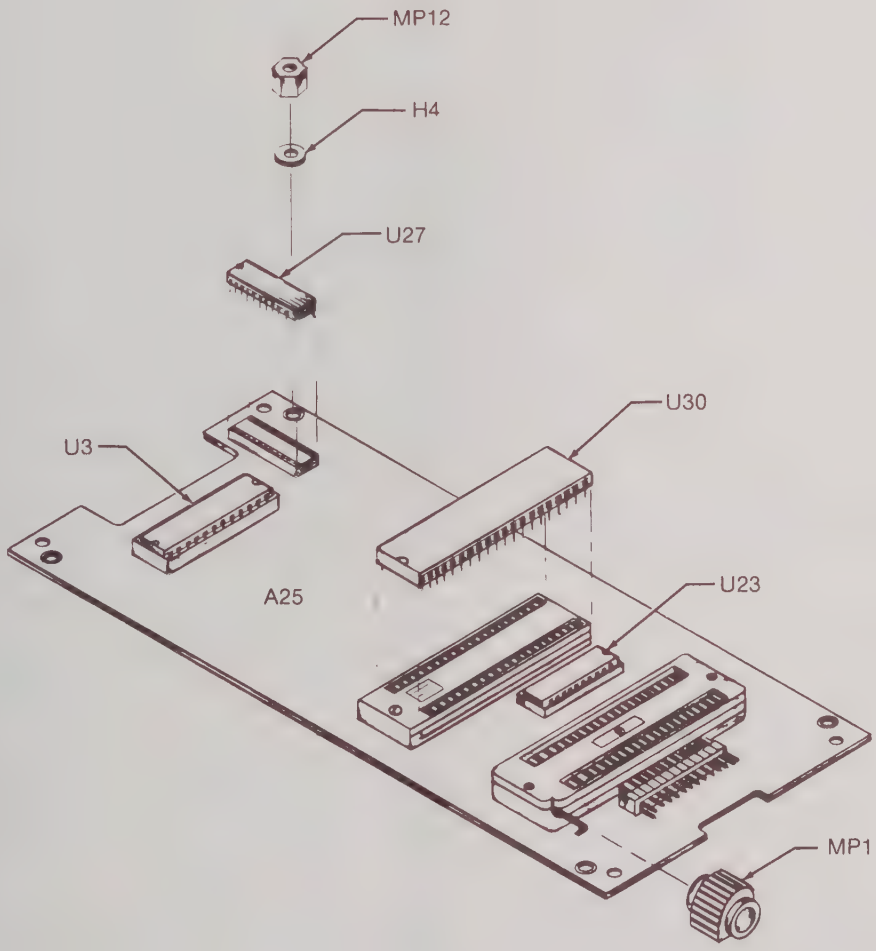


Figure 7-1. 9000A-8048 Final Assembly



DETAIL "A"

9000A-8048-5001
(2 of 2)

Figure 7-1. 9000A-8048 Final Assembly (cont)

Table 7-2. A25 Processor PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A25Ø	PROCESSOR PCB ASSEMBLY FIGURE 7-2 (9000-8048-4071)	647941	89536	647941	REF		
C1	CAP, CER, 20 PF +/-10%, 500V	106369	56289	561CT2HBA102AE200K	4		
C2	CAP, CER, 20 PF +/-10%, 500V	106369	56289	561CT2HBA102AE200K	REF		
C3	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	2		
C4	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	REF		
C5	CAP, CER, 20 PF +/-10%, 500V	106369	56289	561CT2HBA102AE200K	REF		
C6	CAP, CER, 20 PF +/-10%, 500V	106369	56289	561CT2HBA102AE200K	REF		
C7-C20	CAP,CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	14		
J1	CONNECTOR, RIGHT ANGLE	512590	89536	512590	1		
J2	SOCKET, 40-PIN ZERO-INSERTION-FORCE	585133	89536	585133	1		
J3	SOCKET, DIP, 40-PIN	524124	89536	524124	1		
MP1	COMPONENT HOLDER (NOT SHOWN)	422865	98159	2829-75-2	2		
MP2	STANDOFF, ROUND (NOT SHOWN)	380329	89536	380329	5		
P1	CONNECTOR	267500	00779	87022-1	80		
R1	RES, MTL. FILM, 6.34K +/-1%, 1/8W	267344	91637	CMF556341F	1		
R2	RES, MTL. FILM, 1.43K +/-1%, 1/8W	325662	91637	CMF551431F	1		
R3	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	2		
R4	RES, MTL. FILM, 1.58K +/-1%, 1/8W	344341	91637	CMF551581F	1		
R5	RES, MTL. FILM, 1.96K +/-1%, 1/8W	288423	91637	CMF551961F	1		
R6	RES, MTL. FILM, 549 +/-1%, 1/8W	436469	91637	CMF555490F	1		
R7	RES, DEP. CAR, 39 +/-5%, 1/4W	340836	80031	CR251-4-5P39E	1		
R9	RES, COMP, 4.7K +/-, 1/4W	348821	01121	CB4725	3		
R10	RES, COMP, 4.7K +/-, 1/4W	348821	01121	CB4725	REF		
R11	RES, COMP, 4.7K +/-, 1/4W	348821	01121	CB4725	REF		
R12	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	REF		
S1	SWITCH, DIP 4-POS	408559	00779	435166-2	1		
TP1-TP3	CONNECTOR, TEST POINT	512889	02660	62395	3		
U1Ø	IC, NMOS, 8-BIT MICROCOMPUTER	504563	34649	8039	1	1	
U2	IC, LSTTL, OCTAL D TRANS LTCHS TRI	504514	01295	SN74LS373N	1	1	
U4	IC, LSTTL, QUAD 2-INP AND GATE	393066	01295	SN74LS08N	1	1	
U5	IC, TTL, TRIPLE 3-IN POS NAND GATE	363465	01295	SN7412N	1	1	
U6	IC, LSTTL, DUAL 4-IN NAND GATE	393280	01295	SN74LS20N	1	1	
U7	IC, TTL, QUAD 2-INPUT NAND GATE	654210	89536	SN74LS200	1	1	
U8	IC, LSTTL, HEX INVERTER	393058	01295	SN74LS04N	1	1	
U9	IC, LSTTL, OCTL BUS XCVR W/3-STATE	477406	01295	SN74LS245	2	1	
U10	IC, LSTTL, DUAL JK F/F W/PRST & CLR	412999	01295	SN74LS109N	4	1	
U11	IC, LSTTL, QUAD 2-IN OR GATE	393108	01295	SN74LS32N	2	1	
U12	IC, FTTL, QUAD 2-INPUT AND GATE	650523	07263	74F08PC	1	1	
U13Ø	IC, NMOS, 2K X 8 BIT RAM W/IO & TIMER	536847	34649	P8155-2	1	1	
U14	IC, LSTTL, DUAL EDG/TRIG JK F/F W PRST	414029	01295	SN74LS112N	1	1	
U15	IC, LSTTL, 8-BIT MULTIPLX W/STRB	393173	01295	SN74LS151	1	1	
U16	IC, LSTTL, OCTL BUS XCVR W/3-STATE	477406	01295	SN74LS245	REF		
U17	IC, LSTTL, QUAD 2-INPUT	393041	01295	SN74LS02N	2	1	
U18	IC, LSTTL, DUAL JK F/F W/PRST & CLR	412999	01295	SN74LS109N	REF		
U19	IC, LSTTL, DUAL JK F/F W/PRST & CLR	412999	01295	SN74LS109N	REF		
U20	IC, LSTTL, 8-BIT PAR/OUT SER SHFT REG	408732	01295	SN74LS164N	3	1	

Table 7-2. A25 Processor PCB Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
U21	IC, LSTTL, QUAD 2-INPUT	393041	01295	SN74LS02N	REF		
U22	IC, DUAL DIFFERENTIAL COMPARATOR	647115	18324	NE522N	1	1	
U23	IC, LSTTL, QUAD BUFF GTS @ TRI-ST NOT	472746	01295	SN74LS125AN	1	1	
U24	IC, LSTTL, QUAD 2-IN OR GATE	393108	01295	SN74LS32N	REF		
U25	IC, LSTTL, 8-BIT PAR-OUT SER SHFT REG	408732	01295	SN74LS164N	REF		
U26	IC, LSTTL, 8-BIT PAR-OUT SER SHFT REG	408732	01295	SN74LS164N	REF		
U28	IC, LSTTL, QUAD BFR GTS @ TRI-ST NOT	472746	01295	SN74LS125	1	1	
U29	IC, LSTTL, DUAL JK F/F W/PRST & CLR	412999	01295	SN74LS109N	REF		
XU1	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	2		
XU2	SOCKET, IC, 20-PIN	454421	01295	C932002	5		
XU3	SOCKET, IC, 24-PIN	376236	91506	324-AG39D	1		
XU5	SOCKET, IC, 14-PIN	275527	09922	DILB8P-108	2		
XU9	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU11	SOCKET, IC, 14-PIN	275527	09922	DILB8P-108	REF		
XU13	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	REF		
XU16	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU23	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU27	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU29	SOCKET, IC, 16-PIN	276535	91506	316-AG39D	1		
Y1	CRYSTAL, QUARTZ, 11 MHZ	586628	89536	586628	1	1	
Y2	CRYSTAL, QUARTZ, 3.2 MHZ	513937	89536	513937	1	1	
Z1	RESISTOR NETWORK, 1K	414557	89536	414557	1	1	
Z2	RESISTOR NETWORK, 4.7K	412916	89536	412916	1	1	
Z3	RESISTOR NETWORK, 10K	500876	89536	500876	1	1	

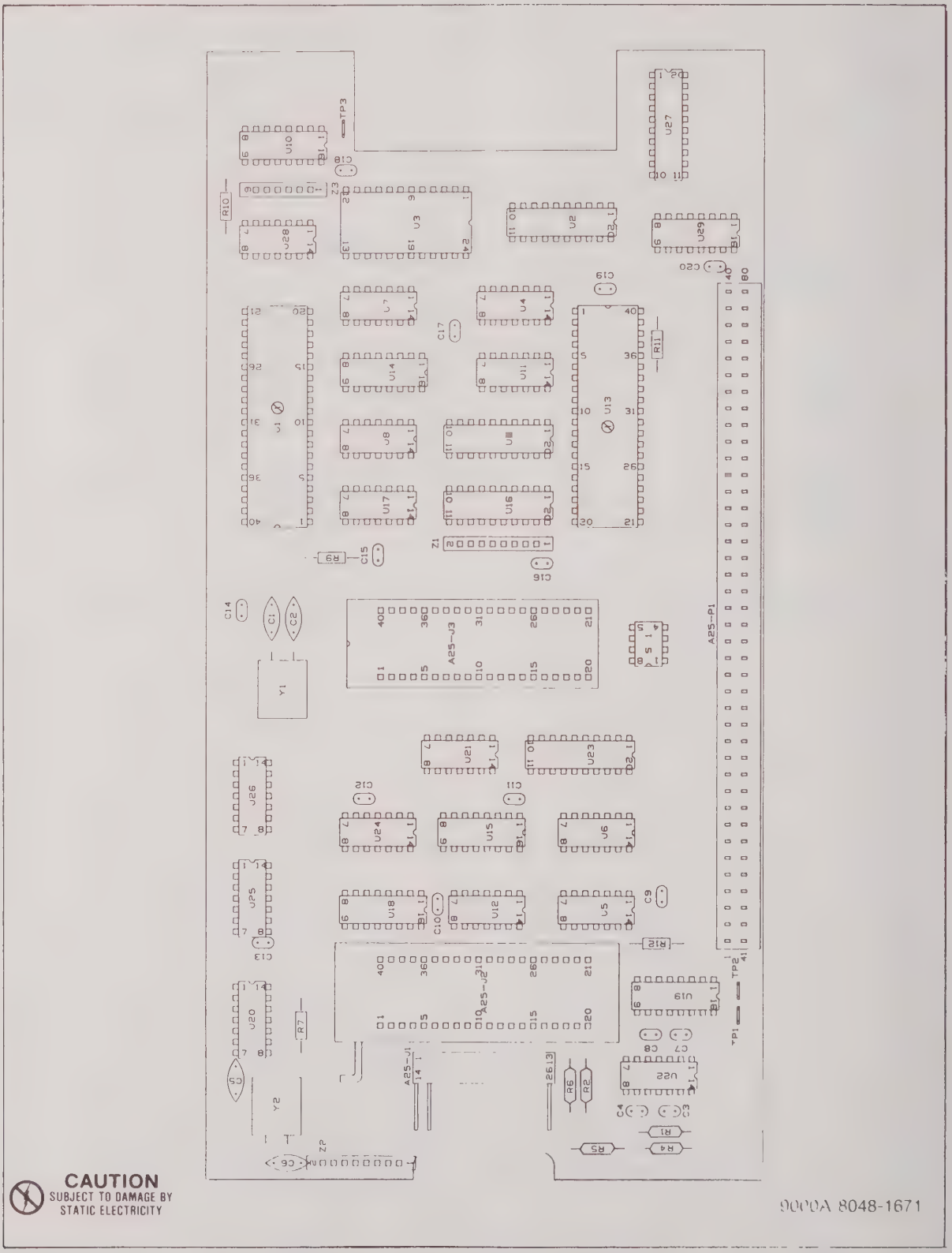


Figure 7-2. A25 Processor PCB Assembly

Table 7-3. A26 Interface PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A26⊗	INTERFACE PCB ASSEMBLY FIGURE 7-3 (9000A-8048-4072)	647958	89536	647958	REF		
A1	HYBRID, PROTECTION 700 TESTED	582189	89536	582189	3	1	
A2	HYBRID, PROTECTION 700 TESTED	582189	89536	582189	REF		
A3	HYBRID, PROTECTION 3K TESTED	582247	89536	582247	2	1	
A4	HYBRID, PROTECTION 3K TESTED	582247	89536	582247	REF		
A5	HYBRID, PROTECTION 700 TESTED	582189	89536	582189	REF		
C1,C2	CAP, ELECT, 10 UF +/-20%, 16V	602326	89536	602326	2		
C3,C4	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	2		
C5-C13	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	30		
C14,C15	CAP, CER, 47 PF +/-2%, 100V	512368	89536	512368	2		
C16-C20	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C21	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	2		
C22	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C23	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015KA1	REF		
C24-C38	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
CR1	DIODE, SI, HOT CARRIER	313247	28484	HP5082-6264	1	1	
CR2-CR4	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	3	1	
J1	CONNECTOR, 80-POSITION	602805	00779	86396-B	1		
J3	CONNECTOR, TERMINAL	267500	00779	87022-1	80		
Q1	TRANSISTOR, SI, NPN	454231	04713	BRF90	1	1	
Q2,Q3	TRANSISTOR	659417	04713	BRF96	2	1	
Q4	TRANSISTOR, SI, NPN	330803	04713	MPS6560	1	1	
R1	RES, DEP. CAR, 3K +/-5%, 1/4W	441527	80031	CR251-4-5P3K	1		
R2	RES, DEP. CAR, 820 +/-5%, 1/4W	442327	80031	CR251-4-5P820E	1		
R3	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	2		
R4	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	REF		
R5	RES, DEP. CAR, 200K +/-5%, 1/4W	441485	80031	CR251-4-5P200K	1		
R6	RES, DEP. CAR, 1.6K +/-5%, 1/4	348805	80031	CR251-4-5P1K6	1		
R7	RES, MTL. FILM, 10K +/-1%, 1/8W	168260	91637	CMF551002F	1		
R8	RES, MTL. FILM, 4.75K +/-1%, 1/8W	260679	91637	CMF554751F	1		
R9	RES, MTL. FILM, 3.24K +/-1%, 1/8W	223578	91637	CMF553241F	1		
R10	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	3		
R11	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	REF		
R12	RES, MTL. FILM, 1K +/-1%, 1/8W	168229	91637	CMF551001F	1		
R13	RES, MTL. FILM, 2.43K +/-1%, 1/8W	312637	91637	CMF552431F	1		
R14	RES, DEP. CAR, 16K +/-5%, 1/4W	442376	80031	CR251-4-5P16K	1		
R15	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	REF		
R16	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-45P1K	1		
R17	RES, COMP, 51K +/-5%, 1/4W	376434	80031	CR251-4-5P51K	3		
R18	RES, COMP, 51K +/-5%, 1/4W	376434	80031	CR251-4-5P51K	REF		
R19	RES, COMP, 51K +/-5%, 1/4W	376434	80031	CR251-4-5P51K	REF		
R20	RES, COMP, 10K +/-5%, 1/8W	643940	01121	BB1035	2		
R21	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	4		
R22	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R23	RES, COMP, 150 +/-5%, 1/8W	655092	01121	BB1515	1		
R24	RES, VAR, 200 +/-10%, 1/4W	226050	80031	ET50W201	1		
R25	RES, MTL. FILM, 301 +/-1%, 1/8W	267740	91637	CMF553010F	1		
R26	RES, DEP. CAR, 220 +/-5%, 1/4W	342626	80031	CR251-4-5P220E	1		

Table 7-3. A26 Interface PCB Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
R27,R28	RES, MTL. FILM, 61.9 +/-1%, 1/4W	659052	91637	CMF5561R9F	2		
R29,R30	RES, COMP, 10 +/-10%, 1/8W	321125	01121	BB1001	2		
R31	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R32	RES, MTL. FILM, 15.4 +/-1%, 1/8W	321299	91637	CMF5515R4F	1		
R33	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R34	RES, COMP, 10K +/-5%, 1/8W	643940	01121	BB1035	REF		
TP1,TP2	TERMINAL, TEST POINT	512889	02660	62395	2		
U1	IC, OCTAL BUS XCVR W/TRI-STATE	647214	01295	SN74ALS245N	2	1	
U2	IC, LSTTL, OCTL D XPRNT LTCHS TRI-ST	504514	01295	SN74LS373N	1	1	
U3-U9⊘	IC, CMOS, OCTL D F/F W/TRI-STATE	585364	36665	74SC374A	7	2	
U10	IC, LSTTL, 3 TO 8 BIT DCDR W/ENAB	407585	01295	SN74LS138N	1	1	
U11⊘	IC, CMOS, TRI-2BIT TO 1BIT MUX/DEMUX	375808	02735	CD4053BE	2	1	
U12	IC, LSTTL, SYNCHRNS 4-BIT UP/DWN CNTR	393223	01295	SN74LS192N	1	1	
U13	IC, LSTTL, QUAD BUFFER GATES EA TRI-ST	585273	01295	SN74LS126N	1	1	
U14	IC, TTL, QUAD 2-INPUT NAND GATE	654210	12040	DM74LS00N	1	1	
U15	IC, LSTTL, QUAD BUFFER GATE @ TRI-ST NOT	472746	01295	SN74LS125AN	2	1	
U16	IC, LSTTL, QUAD 2-INPUT AND GATE	393066	01295	SN74LS08N	2	1	
U17	IC, LSTTL, QUAD BUFFER GATE @ TRI-ST NOT	472746	01295	SN74LS125AN	REF		
U18	IC, OCTAL BUS XCVR W/TRI-STATE	647214	01295	SN74ALS245N	REF		
U19⊘	IC, TTL, TRI-2BIT TO 1BIT MUX/DEMUX	375808	02735	CD4053BE	REF		
U20	IC, LSTTL, QUAD 2-INPUT	393041	01295	SN74LS02N	1	1	
U21	IC, LSTTL, QUAD 2-INPUT AND GATE	393066	01295	SN74LS08N	REF		
U22	IC, LSTTL, TRIPLE 3-INPUT NOR GATE	393090	01295	SN74LS27N	1	1	
U23	IC, PROTECTION	585992	89536	585992	1	1	
U24	IC, DUAL VOLT COMPARATOR, HI-SPEED	647123	18324	LM319N	1	1	
U25	IC, LIN, NPN, 5-XSTR ARRAY	248906	12040	LM3046N	1	1	
VR1	VOLT REFERENCE, 1.22V BANDGAP	452771	89536	452771	1	1	
W1,W2	WIRE, JUMPER	529701	89536	529701	AR		
XR26	INSULATOR	175125	89536	175125	2		
XU1-XU9	SOCKET, IC, 20-PIN	454421	01295	C932002	10		
XU18	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU23	SOCKET, IC, 18-PIN	418228	91506	318-AG39D	1		
XU24	SOCKET, IC, 14-PIN DIP	276527	09922	DILB8P-108	1		
XVR1	INSULATOR	175125	89536	175125	REF		
Z1,Z2	NETWORK, THICK-FILM RESISTOR	583476	89536	583476	2	1	
Z3	NETWORK, 51K 6-PIN 5 RES RESISTOR	514042	89536	514042	1	1	
Z4							

NOTE: SP1 DESIGNATES SPACE FOR A SPARE IC WHEN NEEDED.

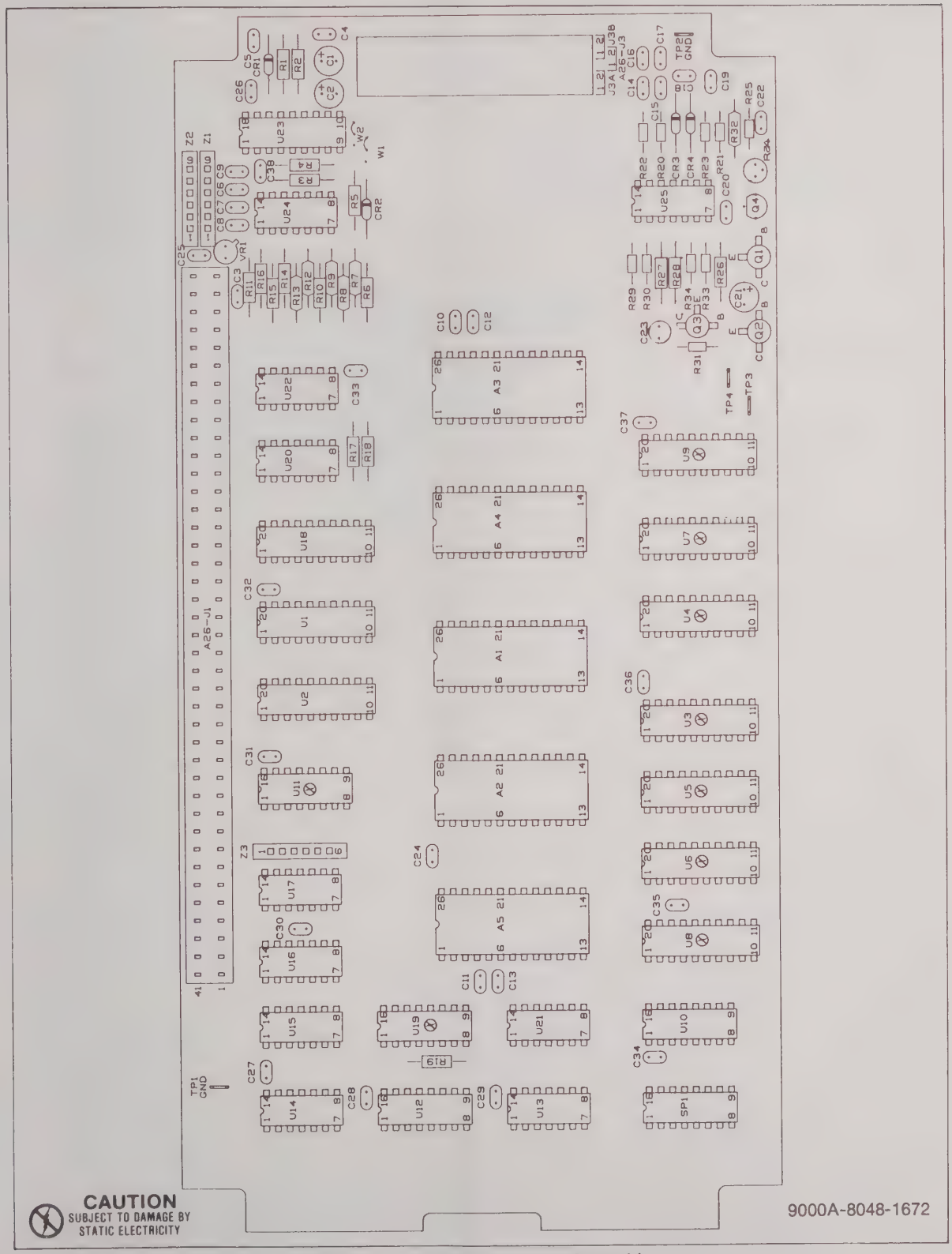


Figure 7-3. A26 Interface PCB Assembly

Table 7-4. Manual Status and Backdating Information

Ref Or Option No.	Assembly Name	Fluke Part No.	* To adapt manual to earlier rev configurations perform changes in desending order (by no.), ending with change under desired rev letter																						
			–	A	B	C	D	E	F	G	H	J	K	L	M	N	P								
A25	Processor PCB Assembly	647941		X																					
A26	Interface PCB Assembly	647958		X																					

* X = The PCB revision levels documented in this manual.
● = These revision letters were never used in the instrument.
–= No revision letter on the PCB.

Section 8
Schematic Diagrams

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8-2.	A26 Interface Assembly	8-5

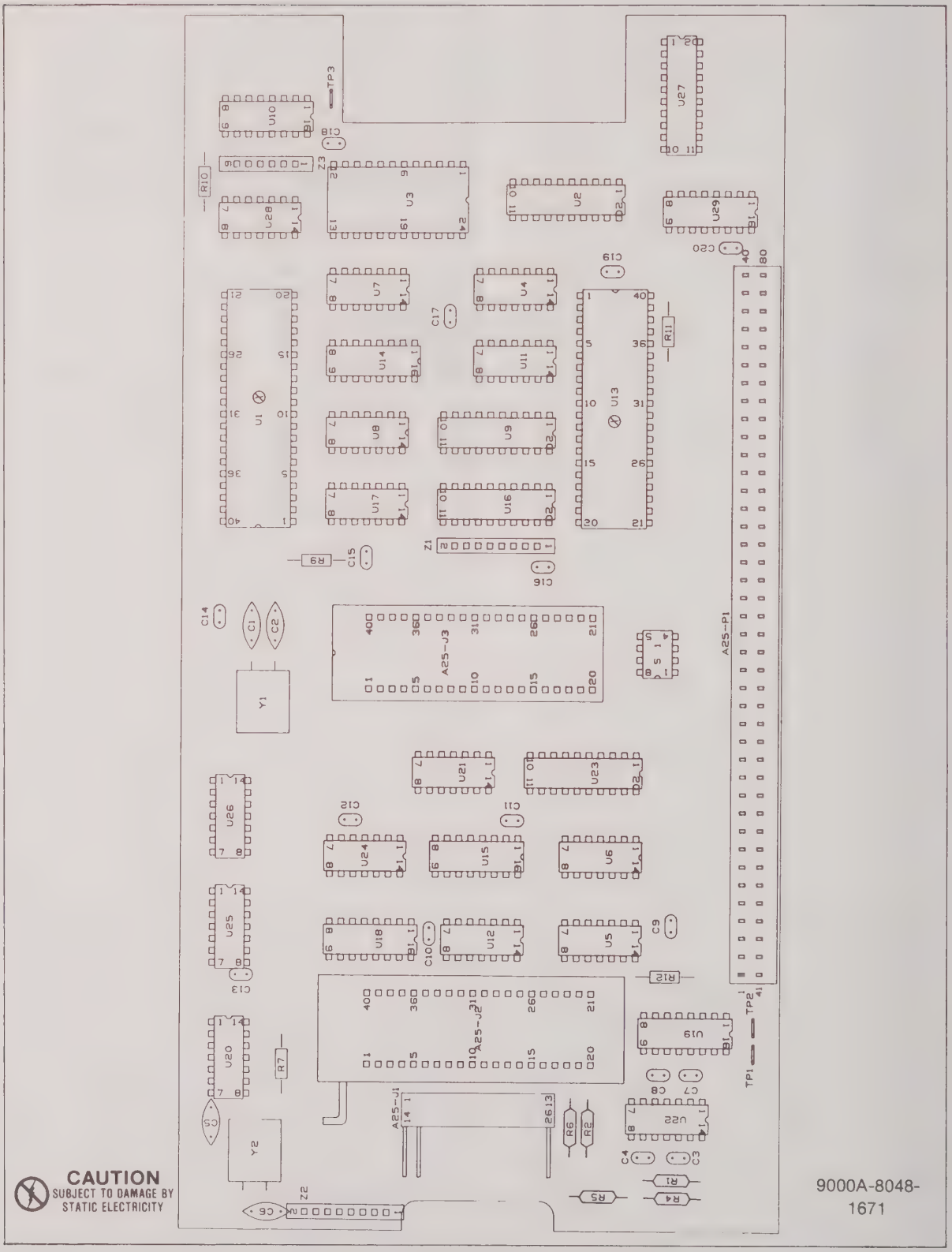
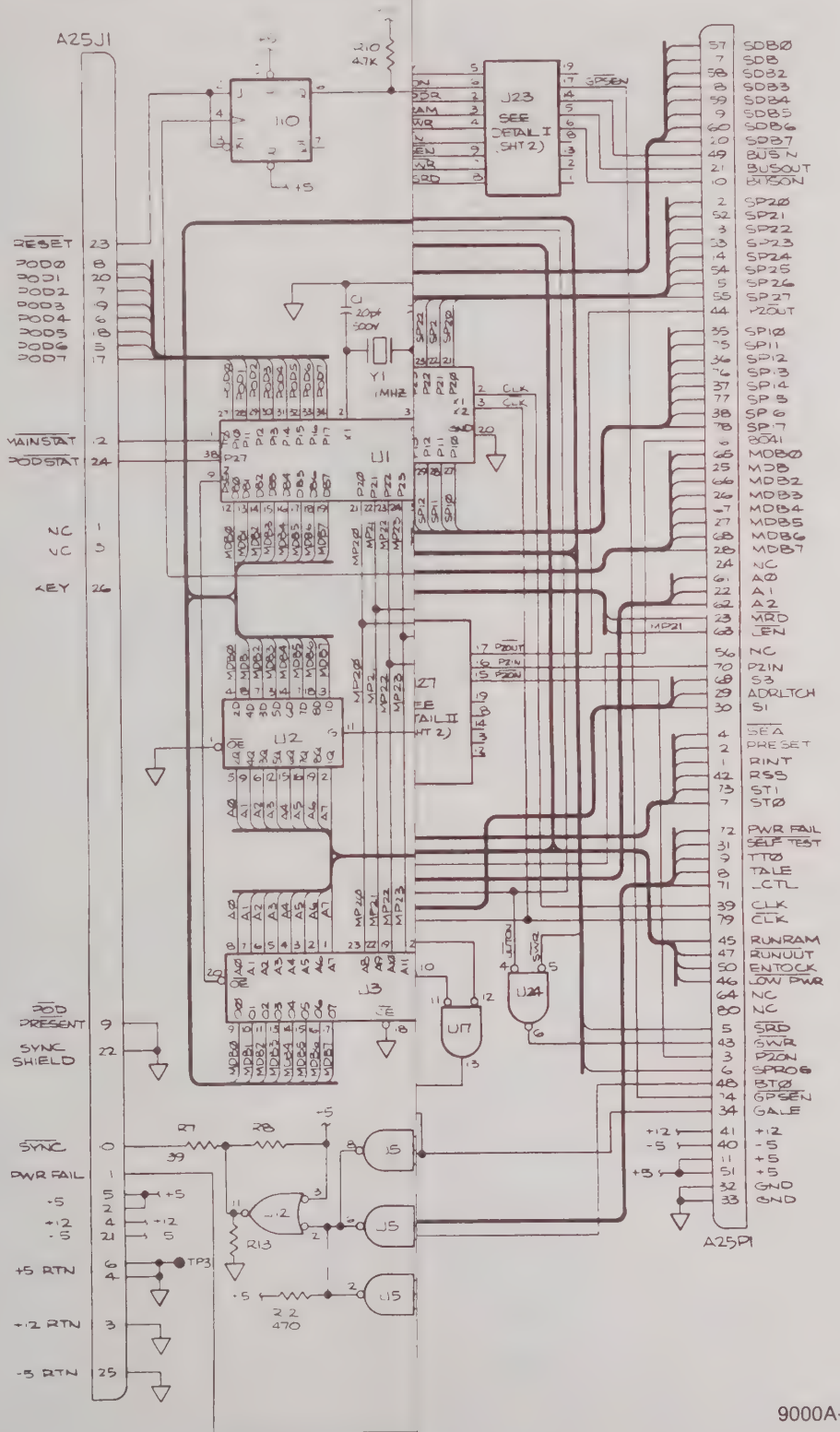


Figure 8-1. A25 Processor PCB Assembly


A25J1
A25P1
U1
U2
U3
U7
U24
J23
SEE DETAIL I (SHT 2)
U5
U6
U7
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U10
U11
U12
U13
U14
U15
U16
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U18
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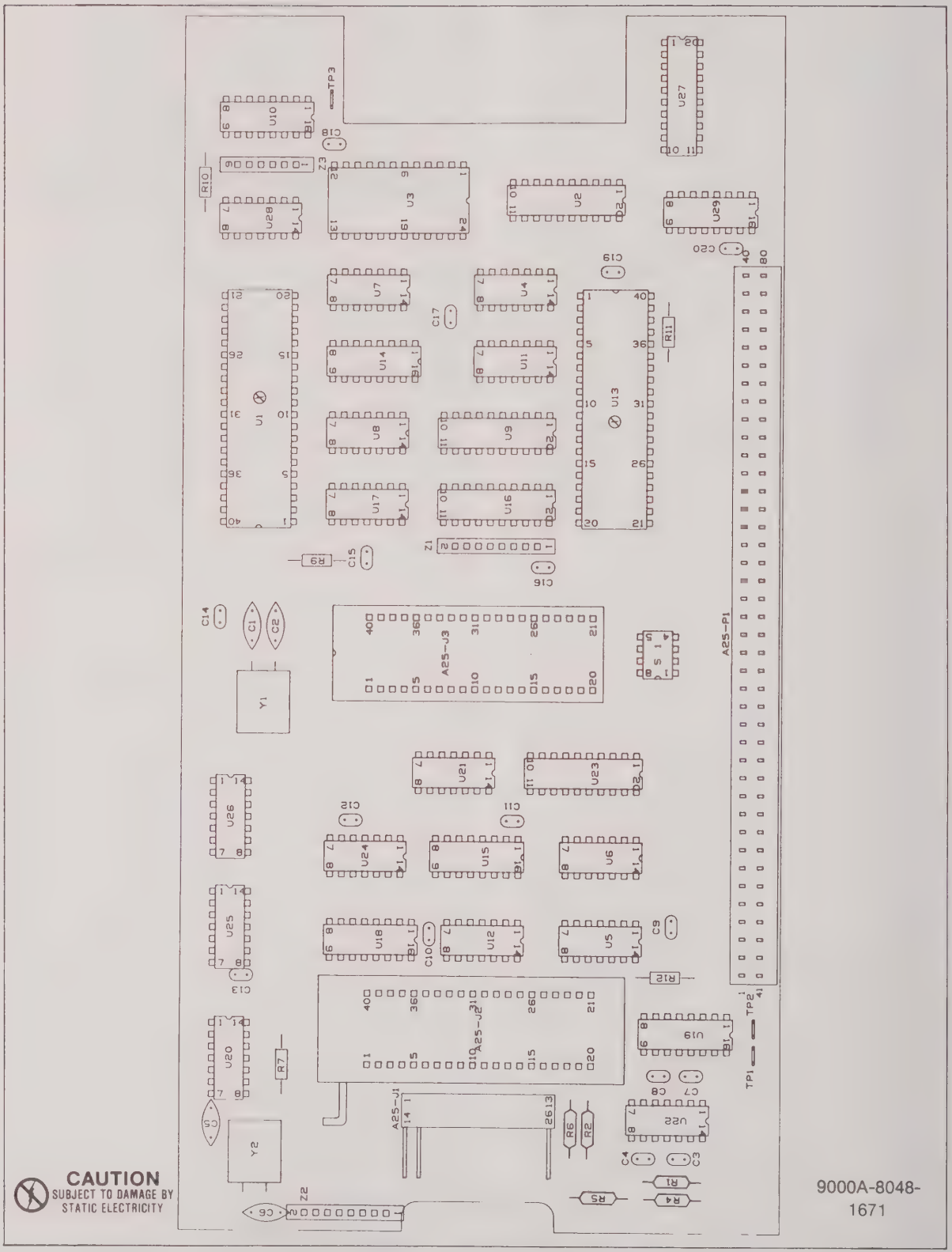
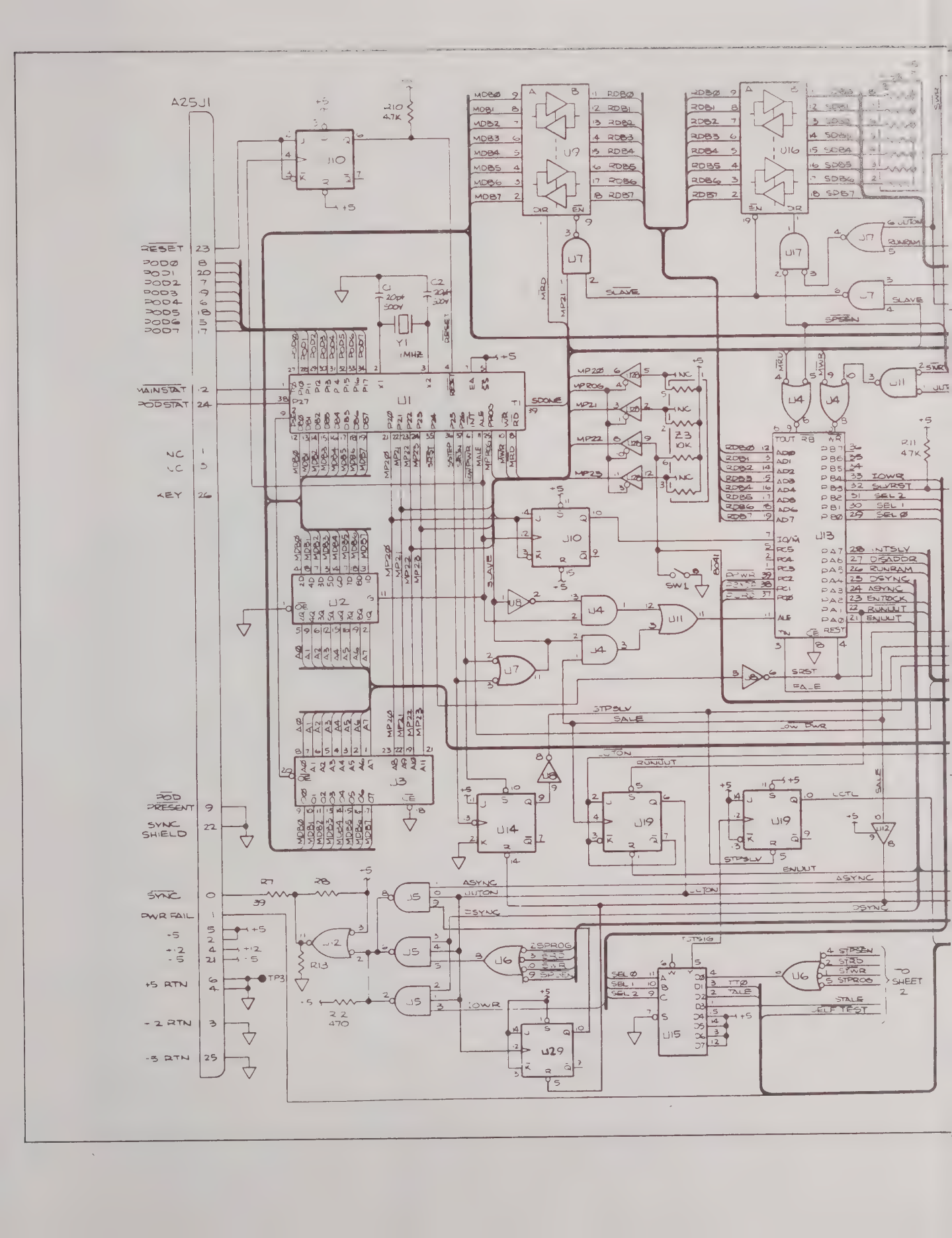


Figure 8-1. A25 Processor PCB Assembly


A25J1
RESET
MAINSTAT
PODSTAT
NC
KEY
POD PRESENT
SYNC SHIELD
SYNC
PWR FAIL
+5
+12
-5
+5 RTN
-2 RTN
-3 RTN
U1
U2
U3
U4
U5
U6
U7
U8
U10
U11
U12
U13
U14
U15
U16
U17
U19
U29
Y1
SW1
SLAVE
SPSEN
STPSLV
SALE
ENUUT
ASYNC
DSYNC
IOWR
SRST
TO SHEET 2

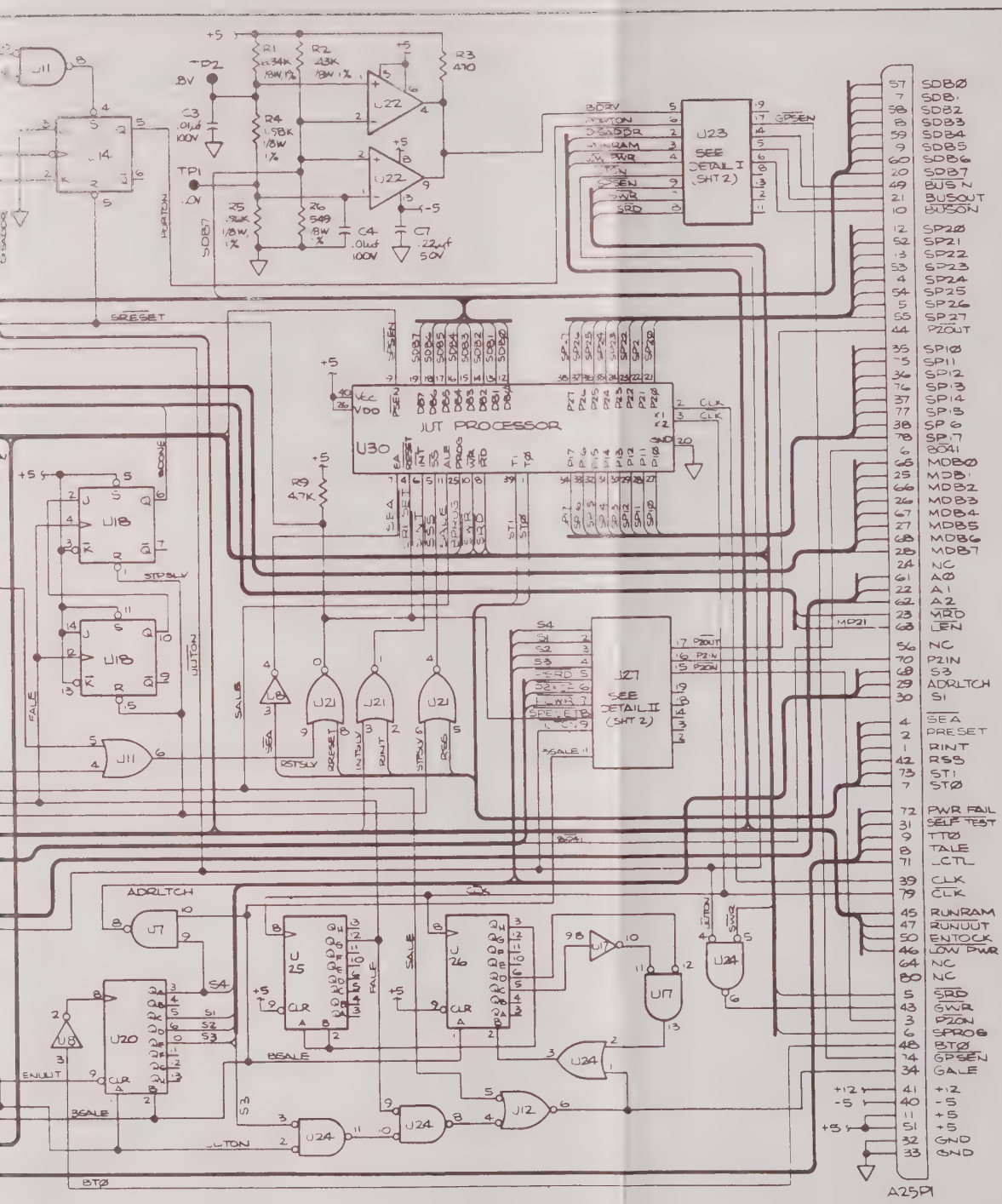


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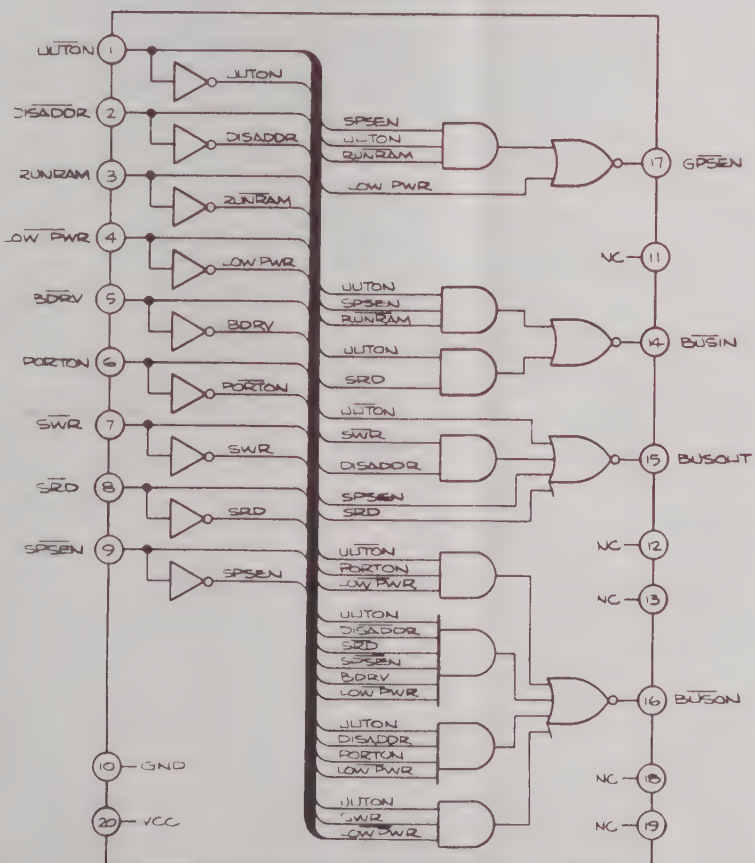
Figure 8-1. A25 Processor PCB Assembly (cont)

DES	DEVICE	+5	GND	PINS	QTY
U1	8039	26,40	20	40	1
U2	74LS373	20	10	20	1
U3	2732	24	12	24	1
U4	74LS08	14	7	14	1
U5	7412	4	7	4	1
U6	74LS20	14	7	14	1
U7	74LS00	14	7	14	1
U8	74LS04	14	7	14	1
U9 U16	74LS245	20	10	20	2
U10 U18 U19, U29	74LS109	16	8	16	4
U11, U24	74LS32	4	7	4	1
U13	8155-2	40	20	40	1
U14	74LS112	16	8	16	1
U15	74LS151	6	8	16	1
U17, U21	74LS02	4	7	14	2
U20, U25, U26	74LS164	14	7	14	3
U22	NE522	14	7	14	1
U23 U27	PAL14L4	20	10	20	2
U28	74LS125	4	7	14	1
Z1	RES. NET. 1K	1	—	8	1
Z2	RES. NET, 4.7K	1	—		1
Z3	RES. NET 10K	1	—	6	1
U12	74F08	14	7	14	1

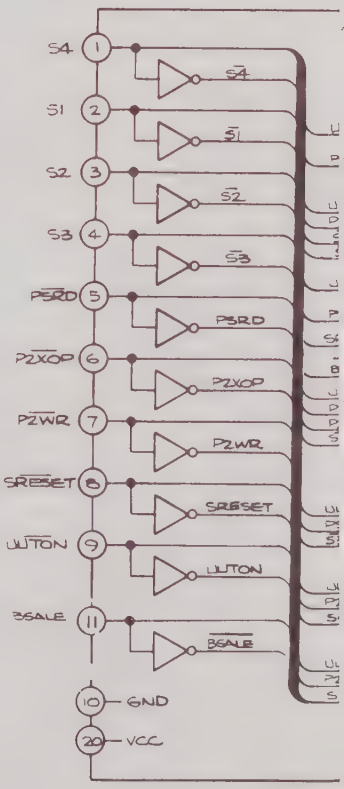
DEVICES ADDRESSABLE BY U1 (8039)

CONTROL	ADDRESS P23-P20	ADDRESS D87 - - - - - D80		DEVICE
PSEN	0000	0000	0000	U3 (2732 EPROM)
	↓	↓	↓	↓
	1111	1111	1111	
RD/WR	XXOX	XXXX	X000	* U4 (74SC374)
	XXOX	XXXX	X001	* U3
	XXOX	XXXX	X010	* U6
	XXOX	XXXX	X011	* U5
	XXOX	XXXX	X100	* U9
	XXOX	XXXX	X101	* U7
	XXOX	XXXX	X110	* U8
	XX10	0000	0000	U13 (8155)
	↓	↓	↓	↓
	XX10	1111	1111	
	XX11	XXXX	X000	
	XX11	XXXX	X001	
	XX11	XXXX	X010	
	XX11	XXXX	X011	
	XX11	XXXX	X100	
	XX11	XXXX	X101	

* DEVICES ON INTERFACE BD #9000A-8048-1072



DETAIL 1
(U23)



DETA
(U2

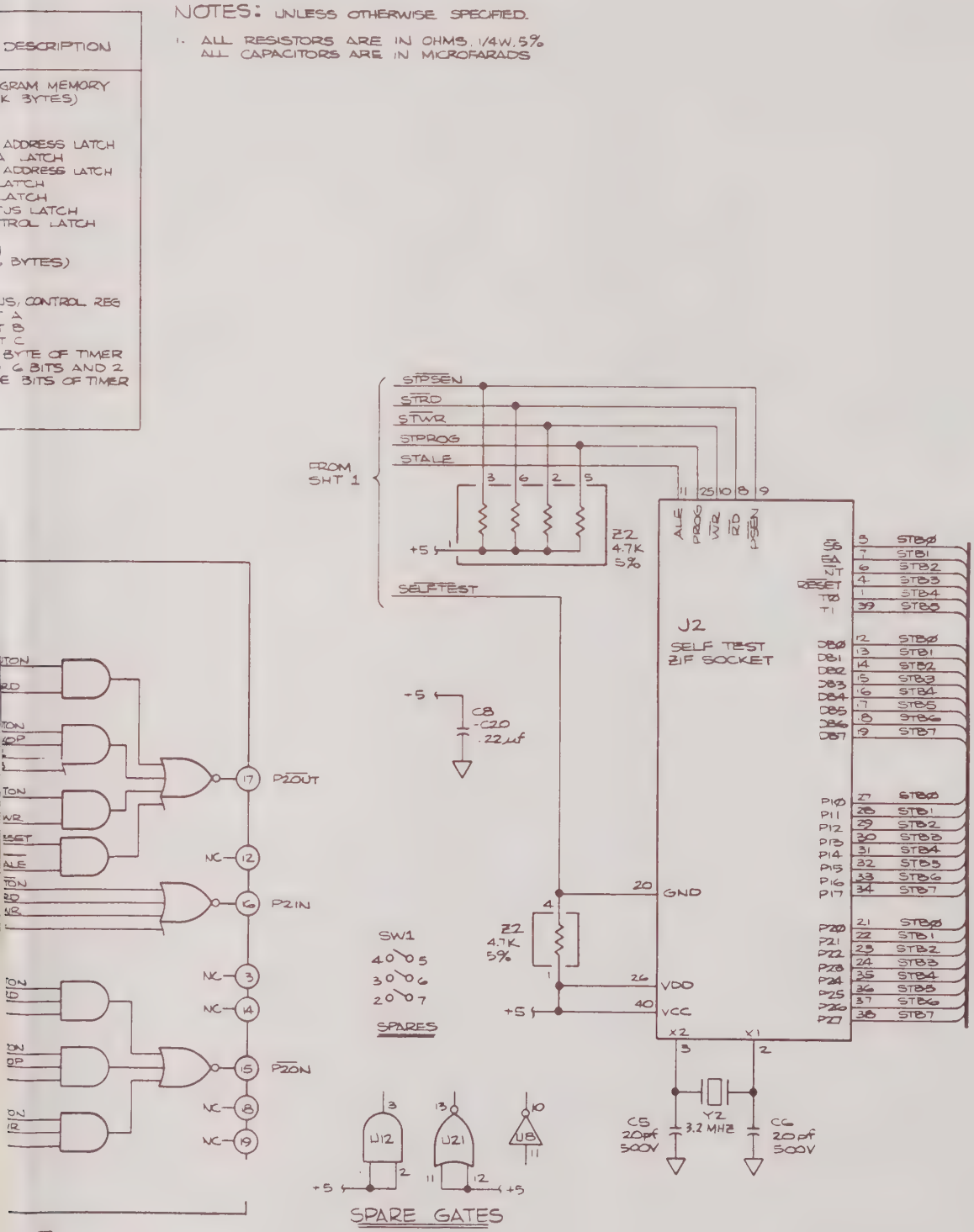


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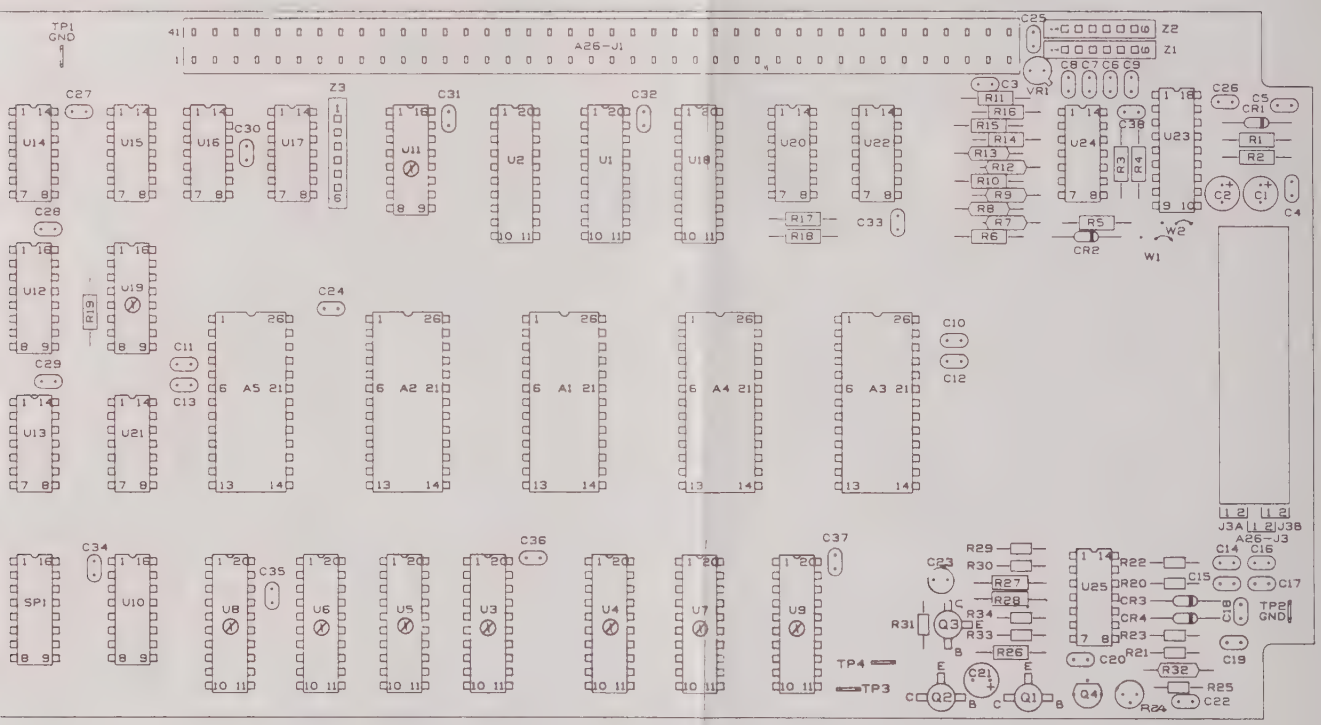
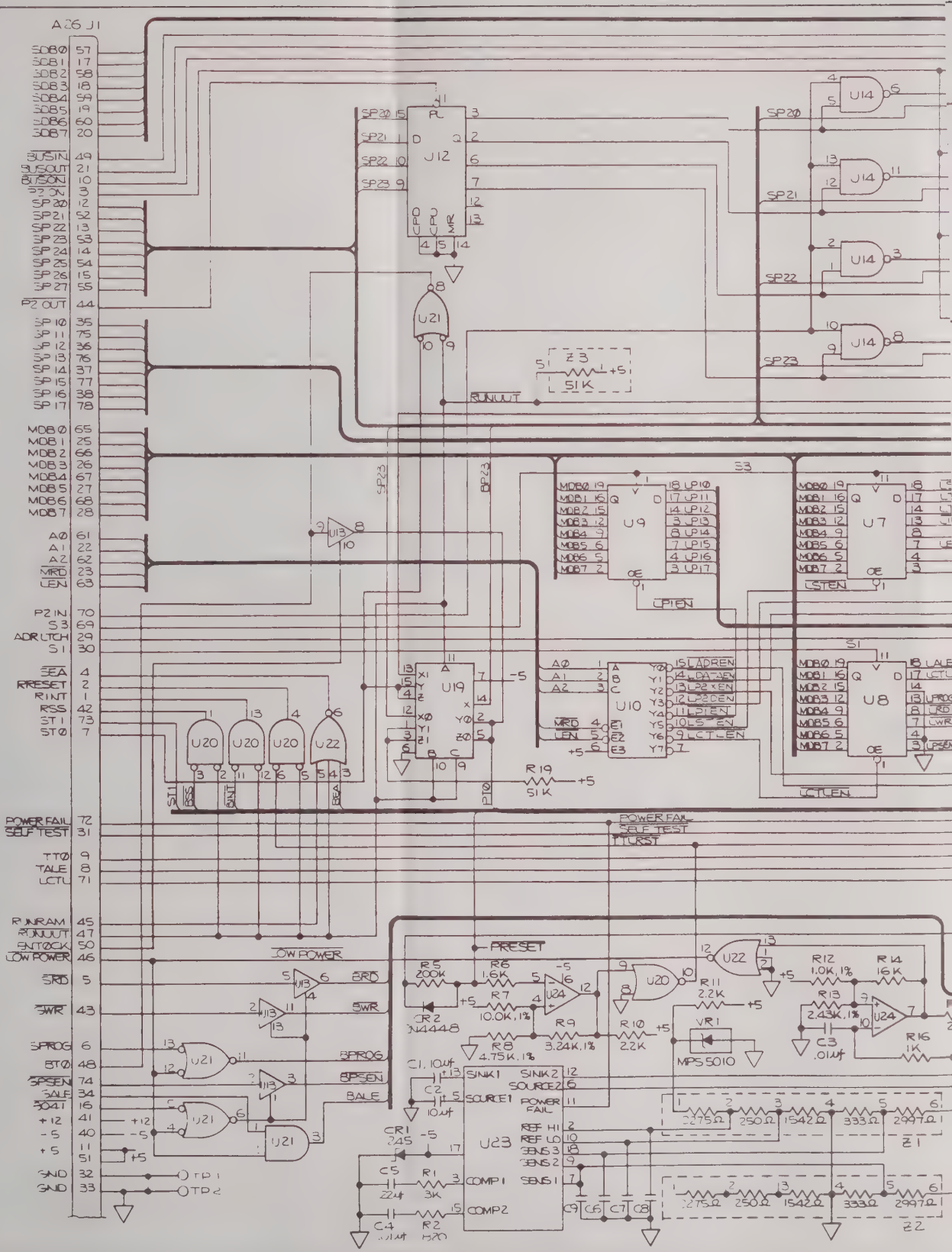
Figure 8-1. A25 Processor PCB Assembly (cont)

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY



9000A-8048-1672

Figure 8-2. A26 Interface PCB Assembly


A26 J1
SDB0 57
SDB1 17
SDB2 58
SDB3 18
SDB4 59
SDB5 19
SDB6 60
SDB7 20
BUSIN 49
BUSOUT 21
BUSON 10
SP20 12
SP21 52
SP22 13
SP23 53
SP24 14
SP25 54
SP26 15
SP27 55
P2 OUT 44
SP10 35
SP11 75
SP12 36
SP13 76
SP14 37
SP15 77
SP16 38
SP17 78
MDB0 65
MDB1 25
MDB2 66
MDB3 26
MDB4 67
MDB5 27
MDB6 68
MDB7 28
A0 61
A1 22
A2 62
MRD 23
LEN 63
P2 IN 70
S3 69
ADR LTCH 29
S1 30
SEA 4
RRESET 2
RINT 1
RSS 42
ST1 73
ST0 7
POWER FAIL 72
SELF TEST 31
TT0 9
TALE 8
LCTL 71
RUNRAM 45
RUNUUT 47
ENTOCK 50
LOW POWER 46
SRD 5
SWR 43
SPROG 6
BT0 48
SPSEN 74
BALE 34
SOUT 16
+12 41
-5 40
+5 11
GND 32
GND 33
U12
U21
U14
Z3
51K
RUNUUT
U9
U7
U13
U19
U20
U22
U10
U8
R19
51K
LPTEN
LCTLEN
LOW POWER
PRESET
U24
U23
R5 200K
R6 1.6K
R7 10.0K, 1%
R8 4.75K, 1%
R9 3.24K, 1%
R10 2.2K
R11 2.2K
R12 1.0K, 1%
R13 2.43K, 1%
R14 16K
R16 1K
VR1
MPS 5010
CR2 1N4448
CR1 245
C1, 10uf
C2 10uf
C3 .01uf
C4 .01uf
C5 22uf
C6
C7
C8
C9
R1 3K
R2 820
SINK1
SINK2
SOURCE1
SOURCE2
POWER FAIL
REF HI
REF LO
SENS 3
SENS 2
SENS 1
COMP 1
COMP 2
2275Ω
250Ω
1542Ω
333Ω
2997Ω
Z1
Z2
TP1
TP2

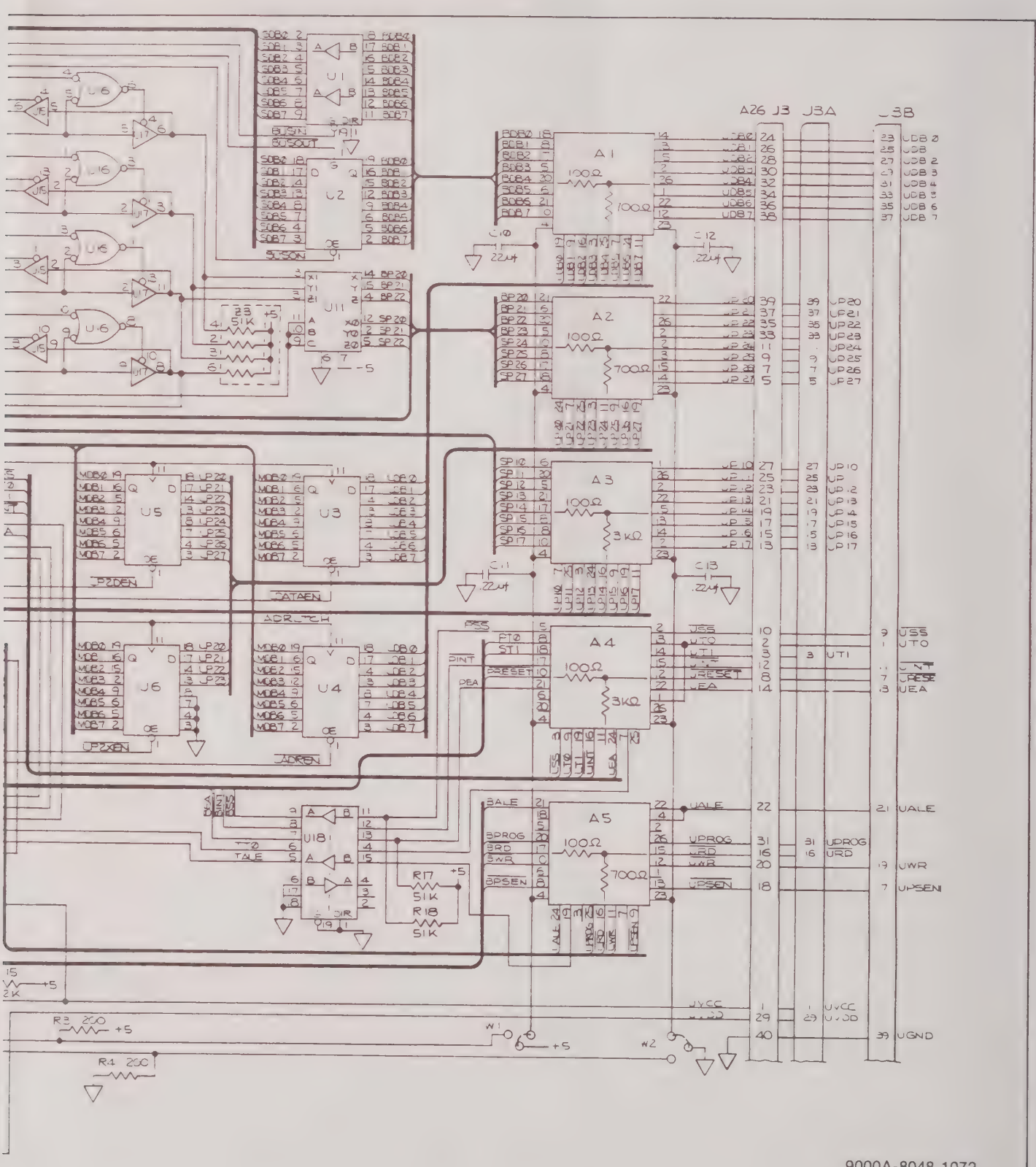


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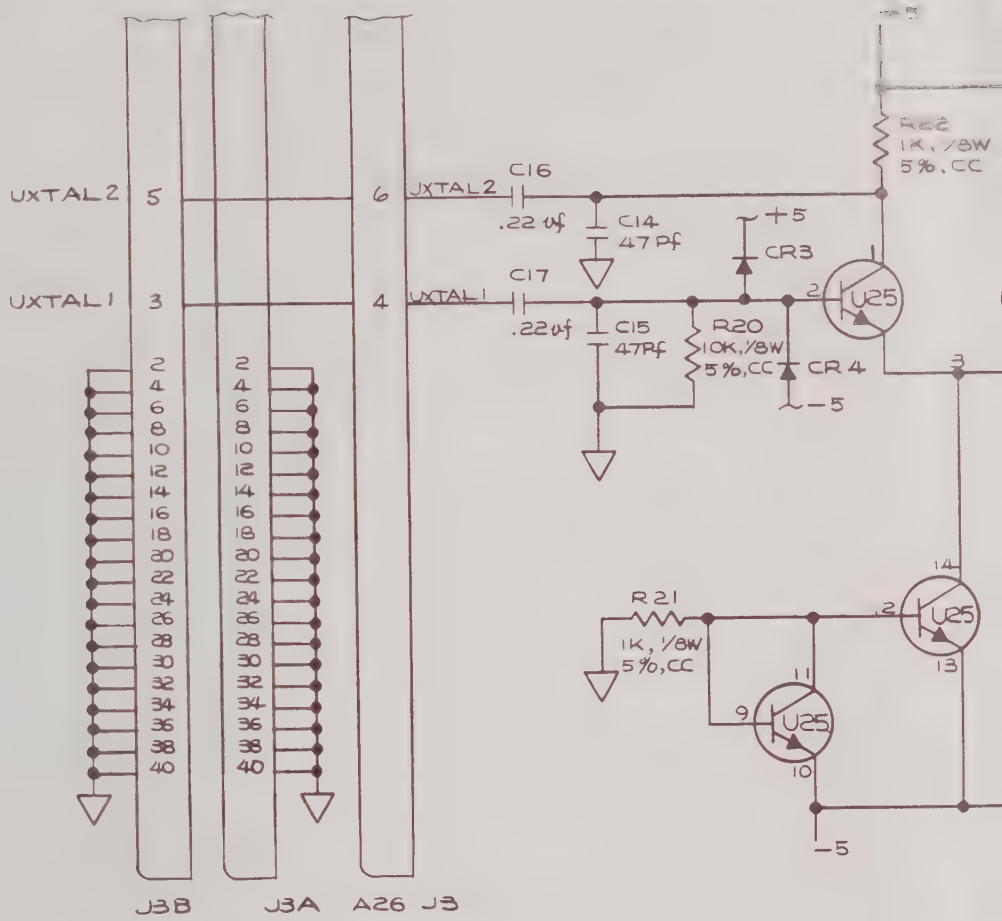
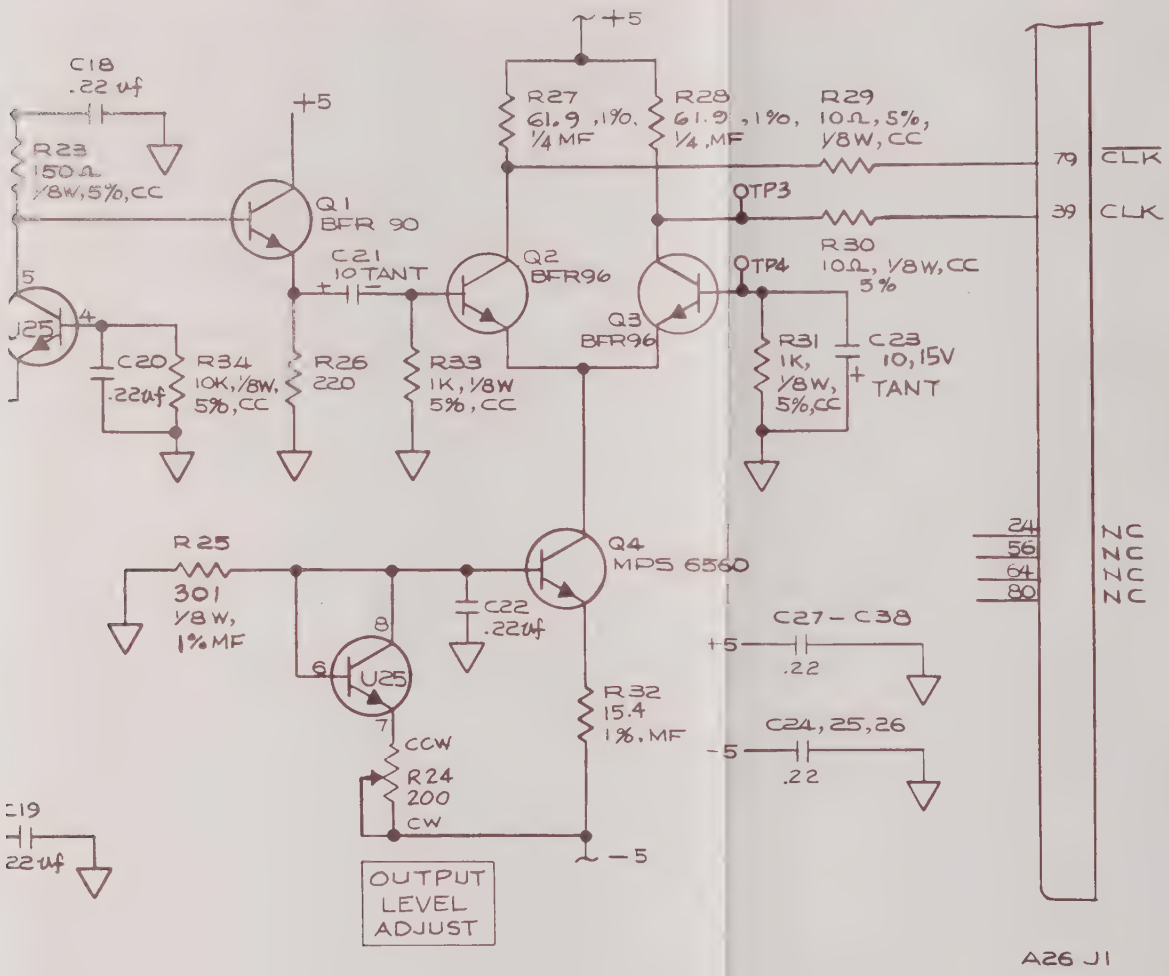
Figure 8-2. A26 Interface PCB Assembly (cont)



DES	DEVICE	+5	GND	PINS	QTY
A1, 2, 5,	9000A-4H02 T	—	—	26	3
A3, 4	9000A-4H01 T	—	—	26	2
U1, 18	74ALS 245	20	10	20	2
U2	74LS 373	20	10	20	1
U3,4,5,6,7,8,9	74SC 374	20	10	20	7
U10	74LS 138	16	8	16	1
U11, 19	4053 B	16	8	16	2
U12	74LS 192	16	8	16	1
U14	74LS 00	14	7	14	1
U15, 17	74LS125	14	7	14	2
U 20	74LS 02	14	7	14	1
U 13	74LS126	14	7	14	1
U 21, 16	74LS 08	14	7	14	2
U 22	74LS 27	14	7	14	1
U 23	3000A-8076	1, 4	8,14,16	18	1
U 24	LM 319	11	3, 8	14	1
U 25	CA 3046	1		6	1
Z 1, 2	54-4087 T	—	4	6	2
Z 3	RES. NETWORK 5K	1	—	6	1



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%, DC.
   ALL CAPACITORS ARE IN MICROFARADS.
2. C6, 7, 8, 9 ARE .22 uf.
3. RESET SCHMITT TRIGGER LEVELS ARE 2.88±.12V AND .92±.12V.
4. LOW POWER SCHMITT TRIGGER LEVELS ARE 3.6±.13V AND 3.4±.14V.

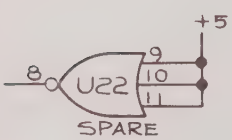


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Figure 8-2. A26 Interface PCB Assembly (cont)

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